Application Report

SNLA140B–May 2004–Revised May 2013

AN-31 Op Amp Circuit Collection

ABSTRACT

This application report provides basic circuits of the Texas Instruments op amp collection.

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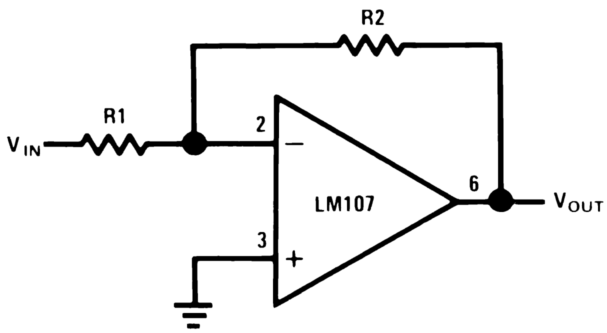
1 Introduction

Texas Instruments recommends replacing 2N2920 and 2N3728 matched pairs with LM394 in all application circuits.

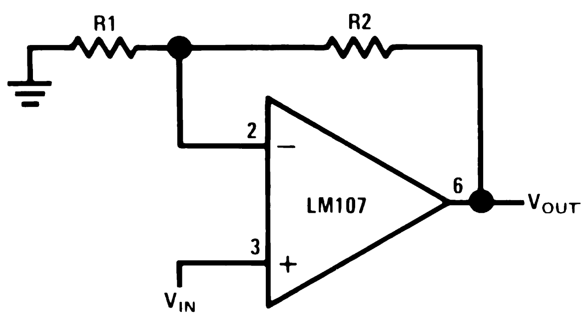
2 Basic Circuits



$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

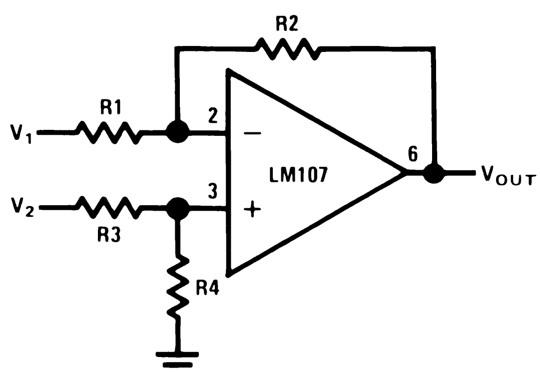
$$R_{IN} = R1$$

Figure 1. Inverting Amplifier



$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

Figure 2. Non-Inverting Amplifier



$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right) \frac{R4}{R1} V_2 - \frac{R2}{R1} V_1$$

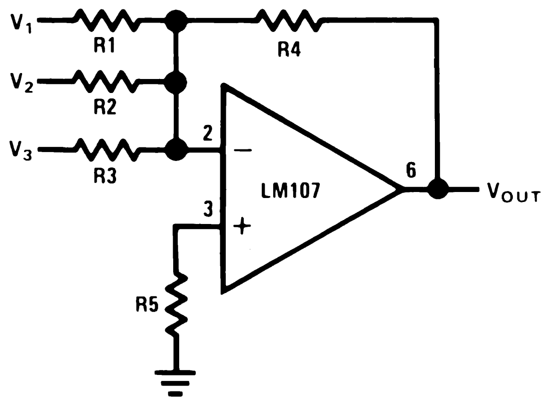
For R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1} (V_2 - V_1)$$

$$R1//R2 = R3//R4$$

For minimum offset error due to input bias current.

Figure 3. Difference Amplifier

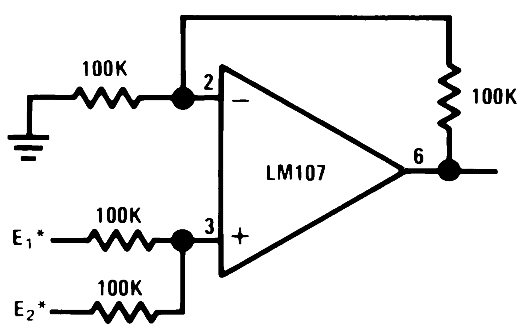


$$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$$

R5 = R1//R2//R3//R4

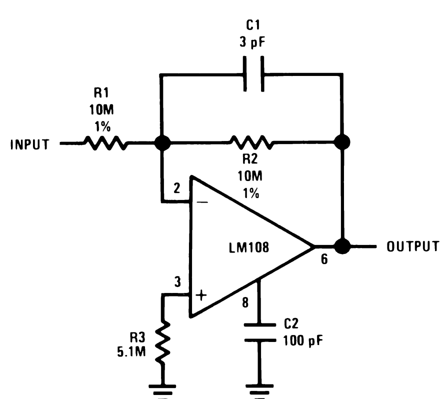
For minimum offset error due to input bias current/

Figure 4. Inverting Summing Amplifier



* R_S = 1k for 1% accuracy

Figure 5. Non-Inverting Summing Amplifier



* Source Impedance less than 100k gives less than 1% gain error.

Figure 6. Inverting Amplifier with High Input Impedance

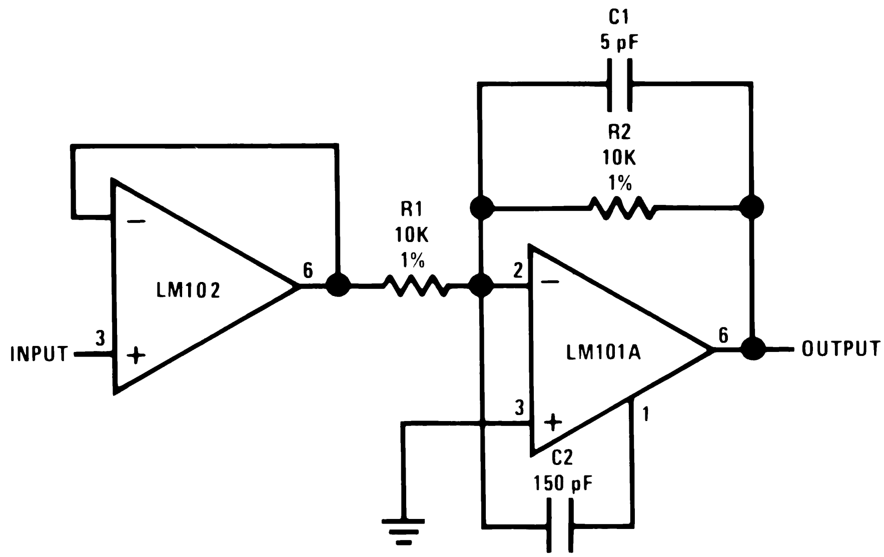
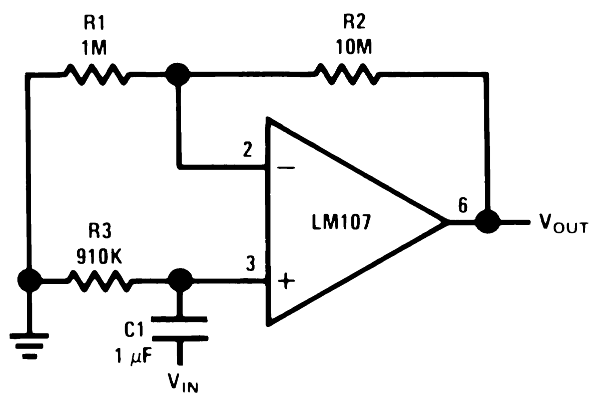


Figure 7. Fast Inverting Amplifier with High Input Impedance

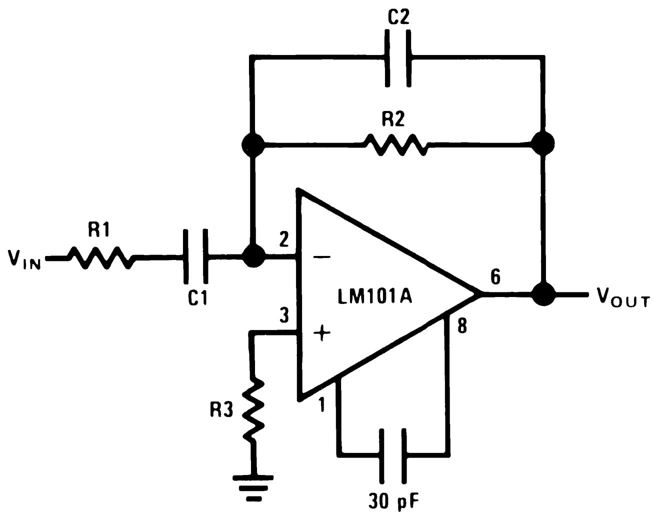


$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

R_{IN} = R3

R3 = R1//R2

Figure 8. Non-Inverting AC Amplifier

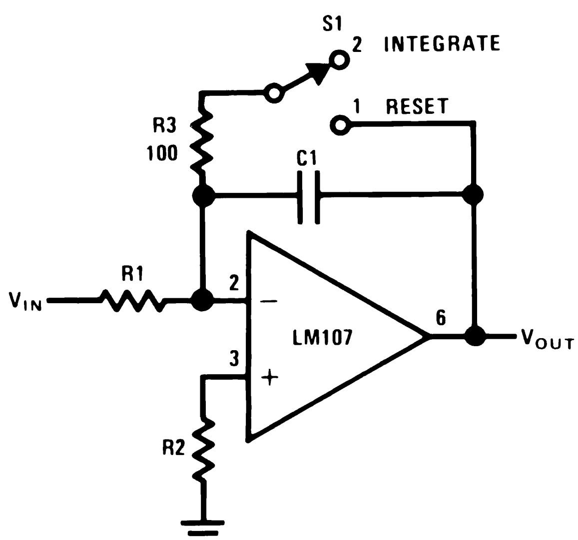


$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$$f_c \ll f_h \ll f_{unity\ gain}$$

Figure 9. Practical Differentiator



$$V_{OUT} = -\frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$$

$$f_c = \frac{1}{2\pi R1C1}$$

$$R1 = R2$$

For minimum offset error due to input bias current.

Figure 10. Integrator

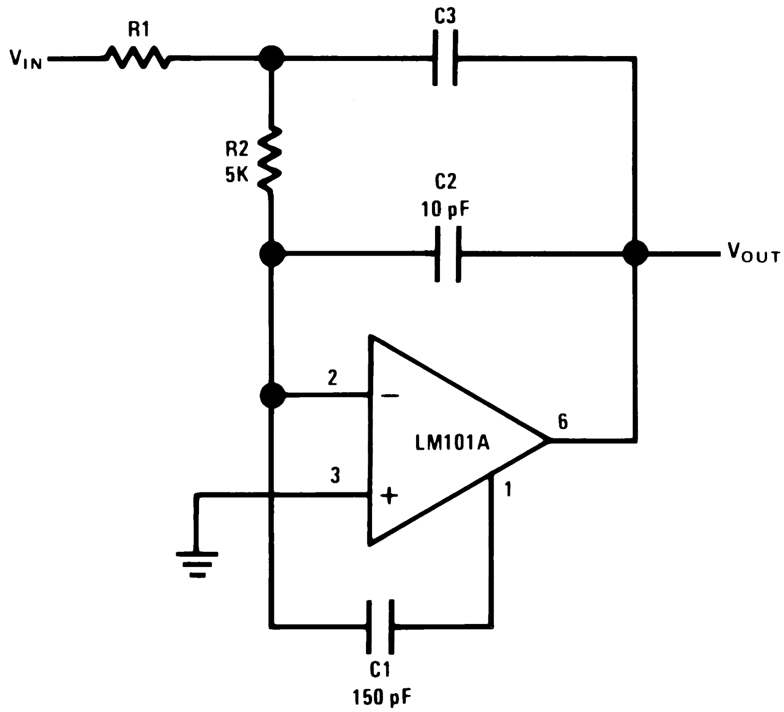
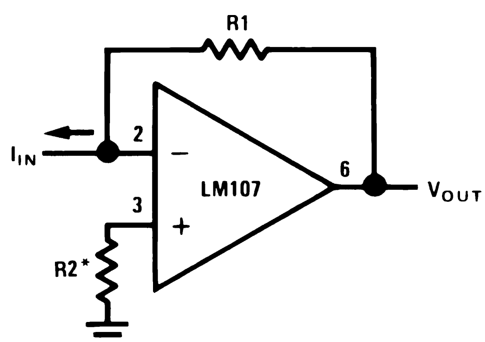


Figure 11. Fast Integrator



$V_{OUT} = I_{IN}$ R1
*For minimum error due to bias current R2 = R1

Figure 12. Current to Voltage Converter

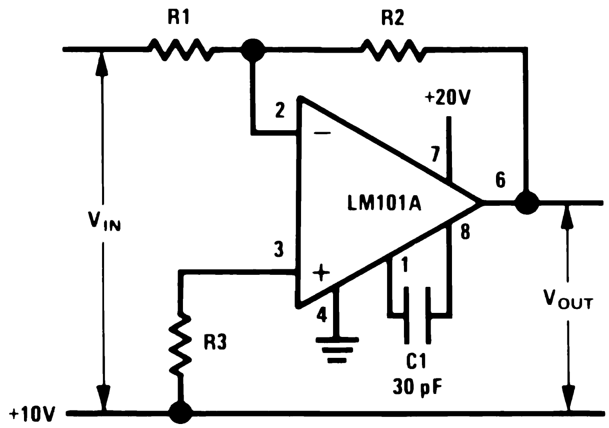


Figure 13. Circuit for Operating the LM101 Without a Negative Supply

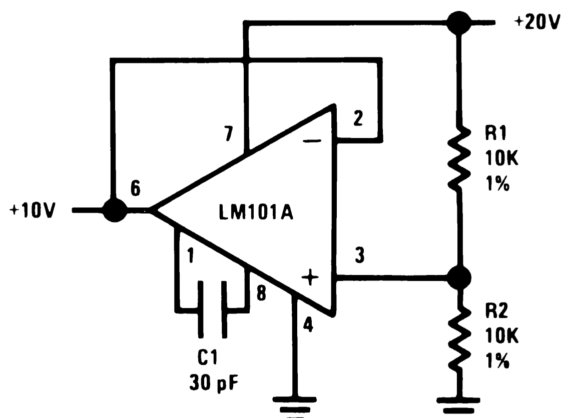


Figure 14. Circuit for Generating the Second Positive Voltage

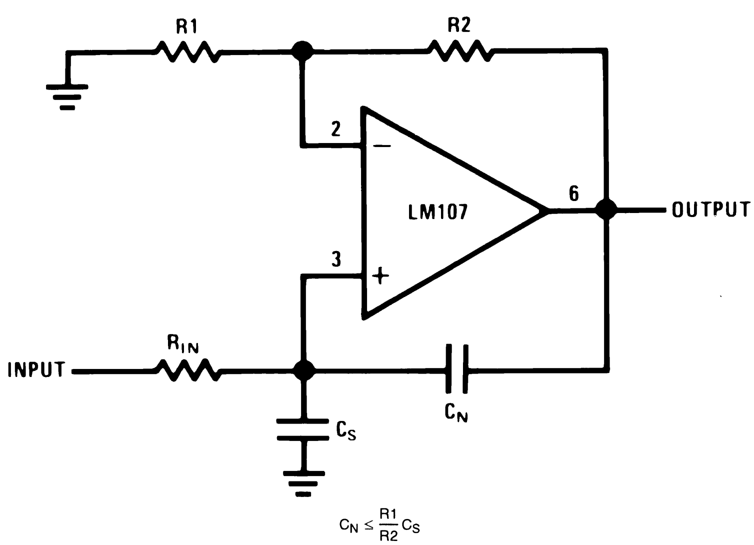
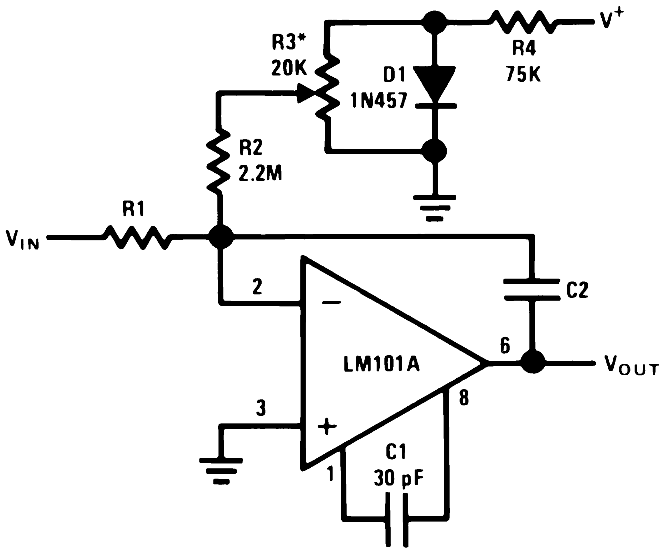


Figure 15. Neutralizing Input Capacitance to Optimize Response Time



* Adjust for zero integrator drift.
Current drift typically 0.1 n/A°C over −55°C to 125°C temperature range.

Figure 16. Integrator with Bias Current Compensation

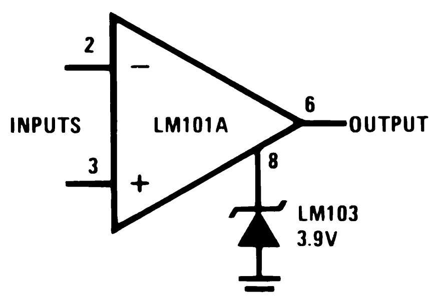


Figure 17. Voltage Comparator for Driving DTL or TTL Integrated Circuits

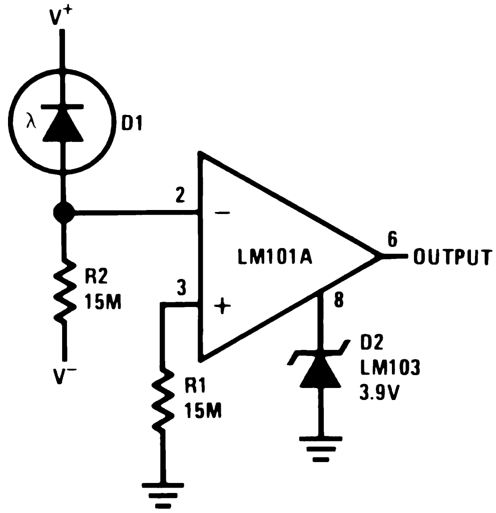
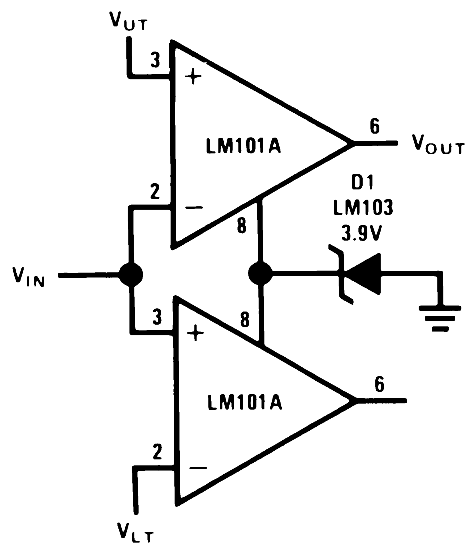


Figure 18. Threshold Detector for Photodiodes



V_{OUT} = 4.6V for $V_{LT} \leq V_{IN} \leq V_{UT}$
V_{OUT} = 0V for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

Figure 19. Double-Ended Limit Detector

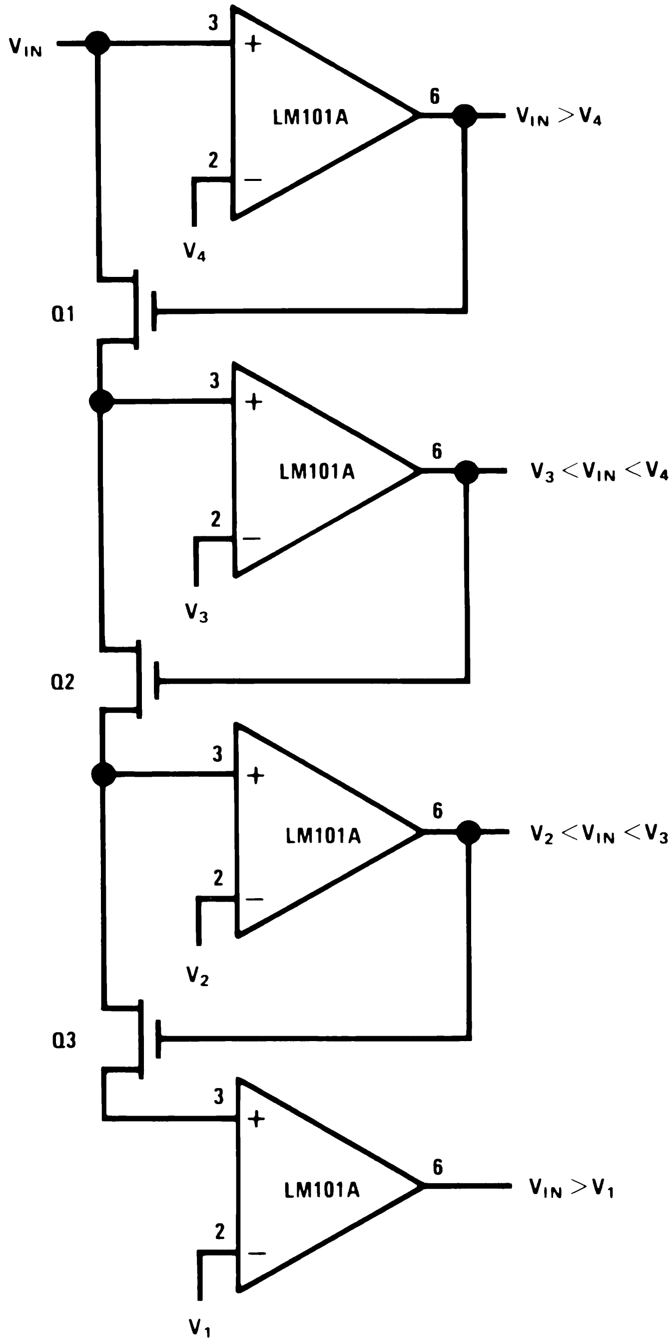
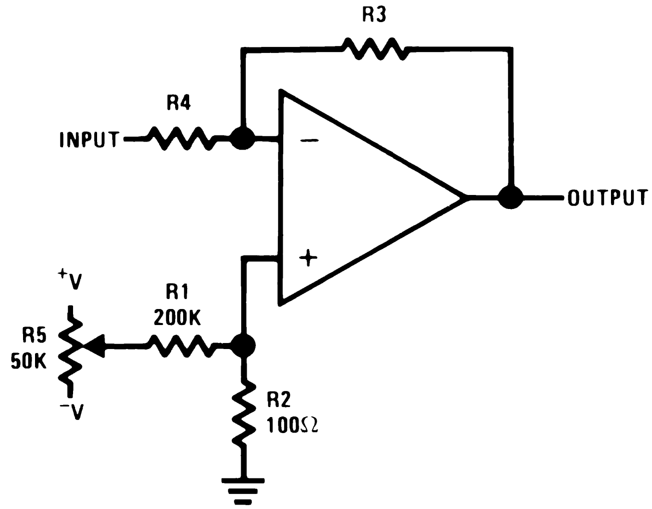
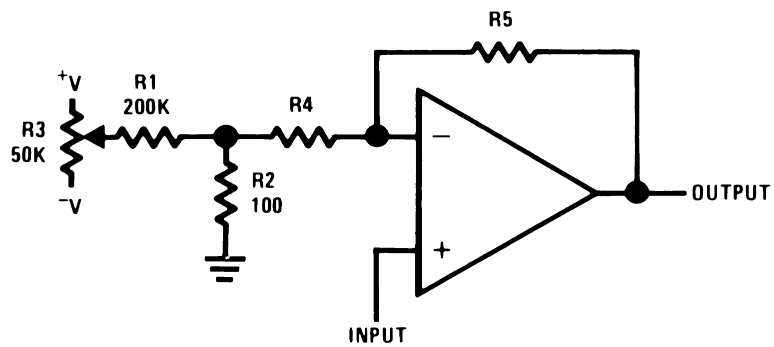


Figure 20. Multiple Aperture Window Discriminator



$$\text{RANGE} = \pm V \left(\frac{R2}{R1}\right)$$

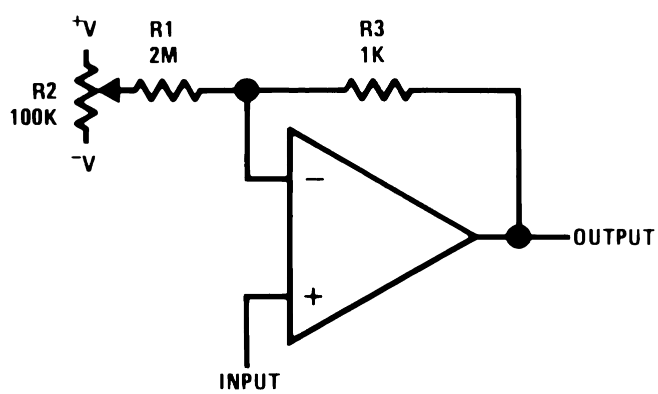
Figure 21. Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element



$$\text{RANGE} = \pm V \left(\frac{R2}{R1}\right)$$

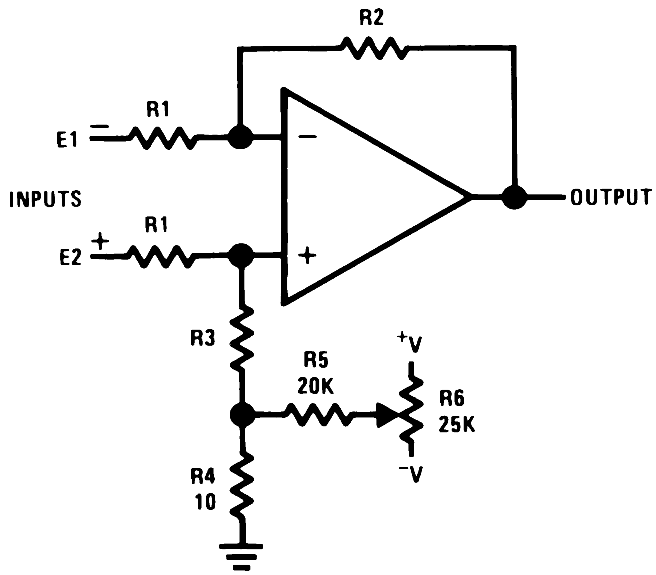
$$\text{GAIN} = 1 + \frac{R5}{R4 + R2}$$

Figure 22. Offset Voltage Adjustment for Non-Inverting Amplifiers Using Any Type of Feedback Element



$$\text{RANGE} = \pm V \left(\frac{R3}{R1}\right)$$

Figure 23. Offset Voltage Adjustment for Voltage Followers

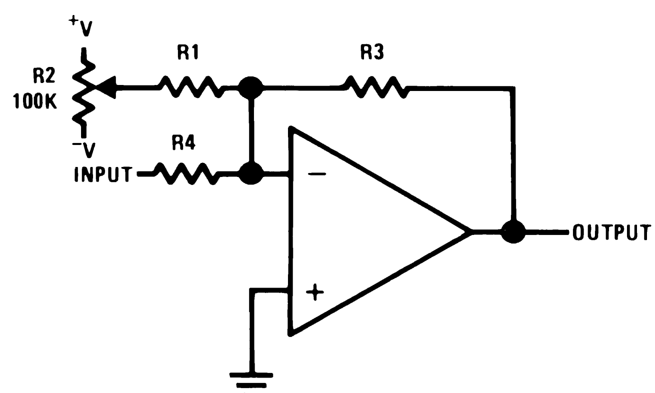


$R2 = R3 + R4$

$RANGE = \pm V \left(\frac{R5}{R4}\right)\left(\frac{R1}{R1 + R3}\right)$

$GAIN = \frac{R2}{R1}$

Figure 24. Offset Voltage Adjustment for Differential Amplifiers



$R1 = 2000\ R3//R4$

$R4//R3 \leq 10\ k\Omega$

$RANGE = \pm V \left(\frac{R3//R4}{R1}\right)$

Figure 25. Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

3 Signal Generation

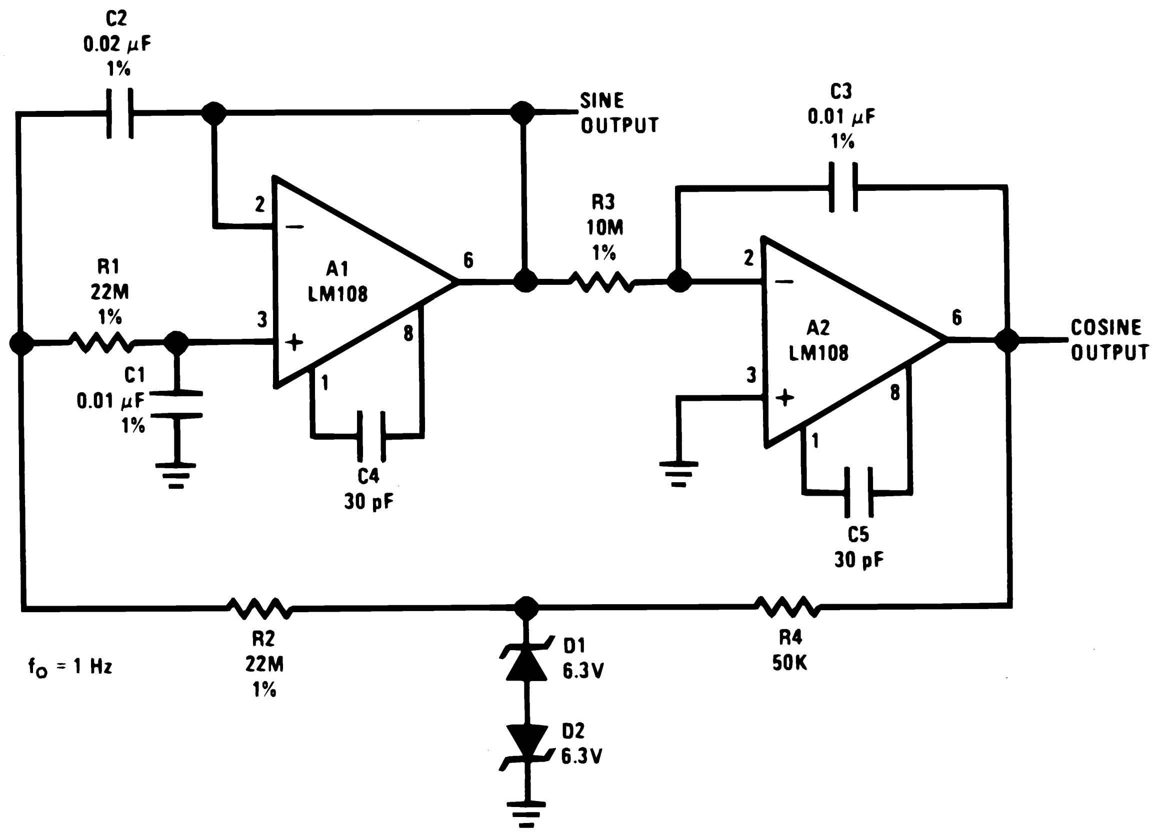


Figure 26. Low Frequency Sine Wave Generator with Quadrature Output

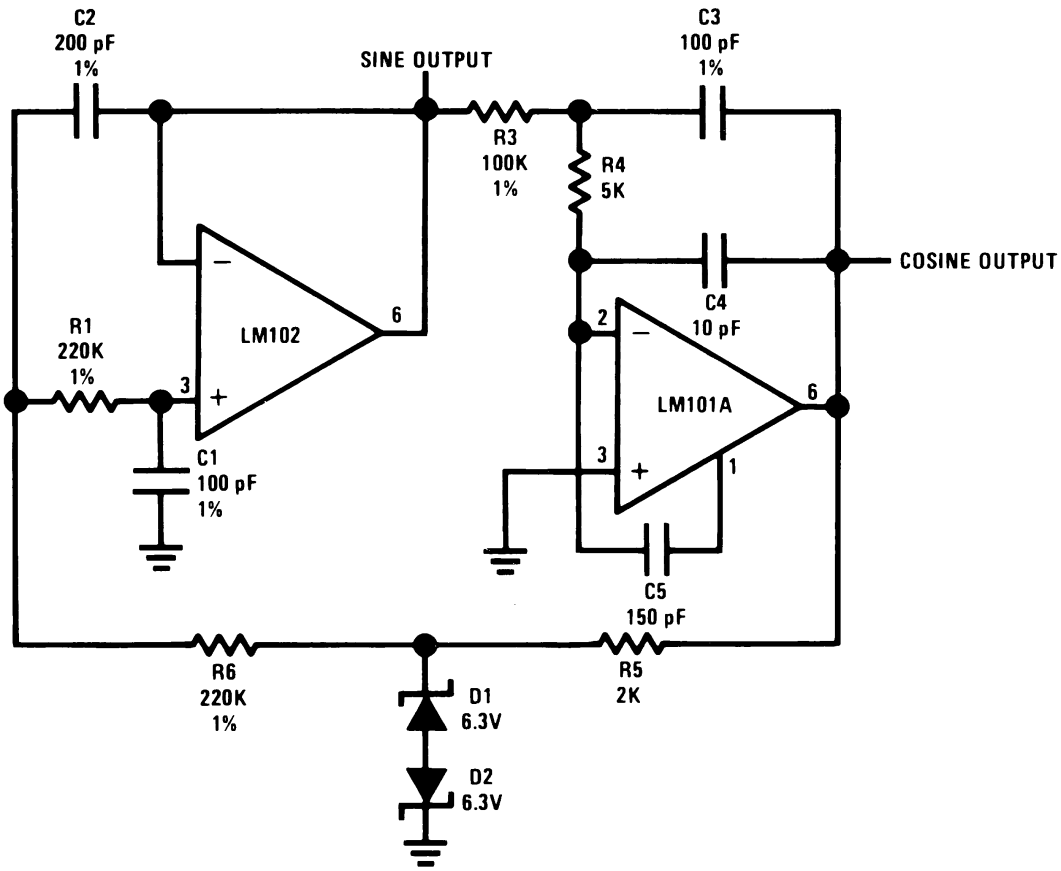
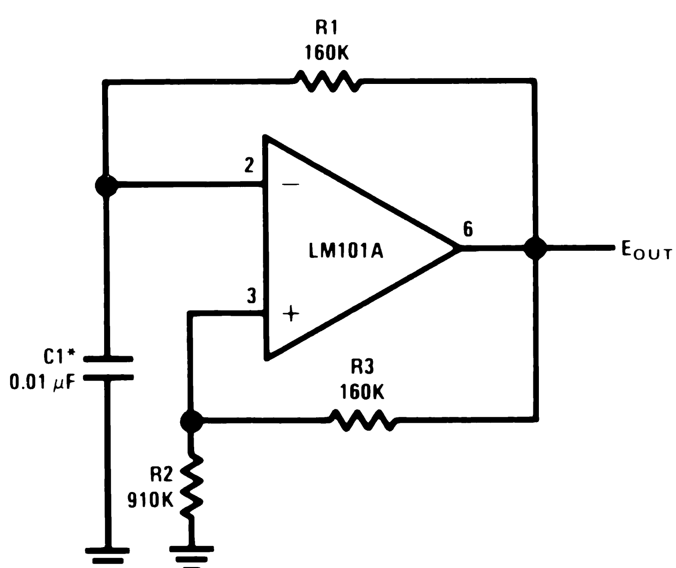
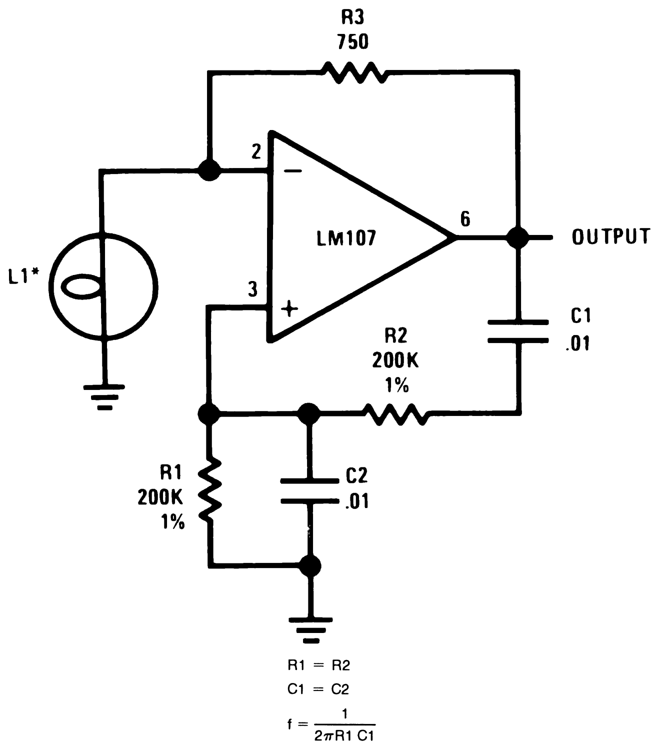


Figure 27. High Frequency Sine Wave Generator with Quadrature Output



* Chosen for oscillation at 100 Hz

Figure 28. Free-Running Multivibrator



* Eldema 1869 10V, 14 mA Bulb

Figure 29. Wein Bridge Sine Wave Oscillator

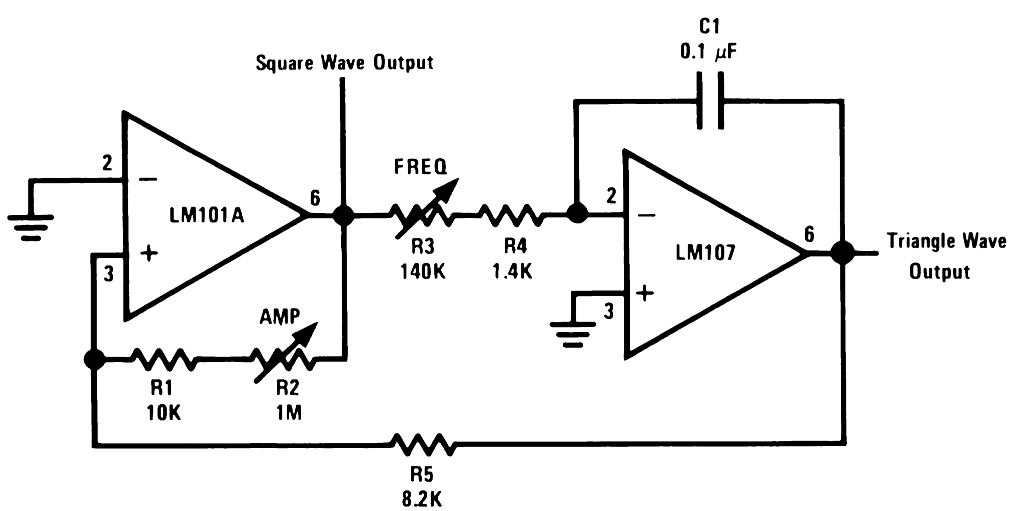


Figure 30. Function Generator

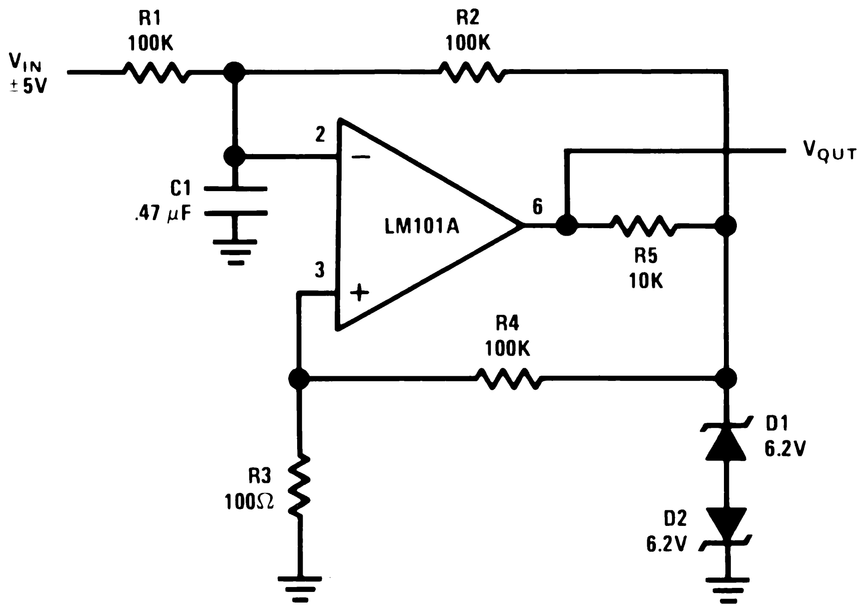
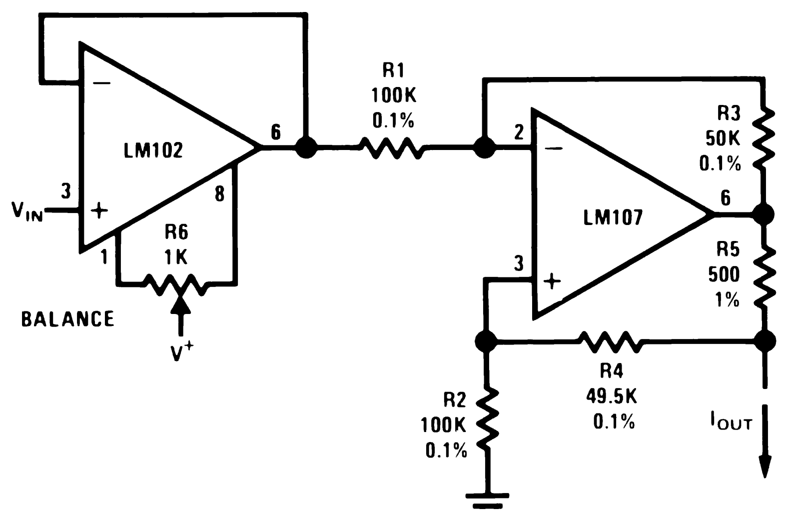


Figure 31. Pulse Width Modulator

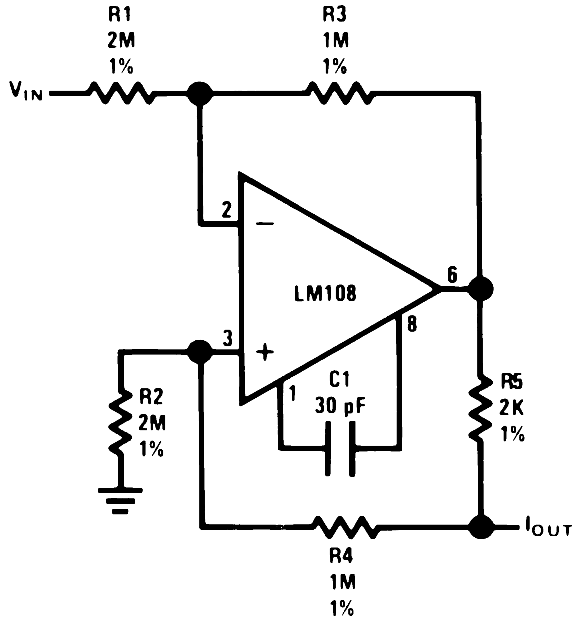


$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

$$R3 = R4 + R5$$

$$R1 = R2$$

Figure 32. Bilateral Current Source



$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

$$R3 = R4 + R5$$

$$R1 = R2$$

Figure 33. Bilateral Current Source

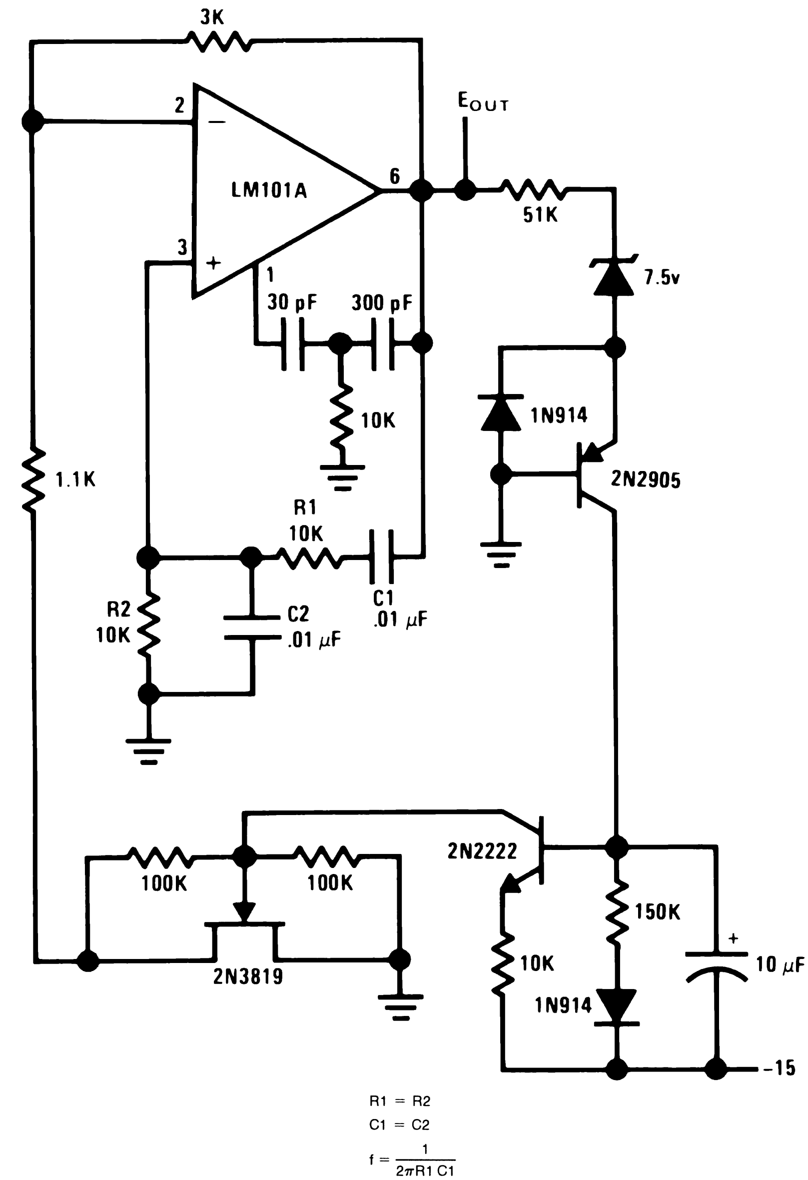
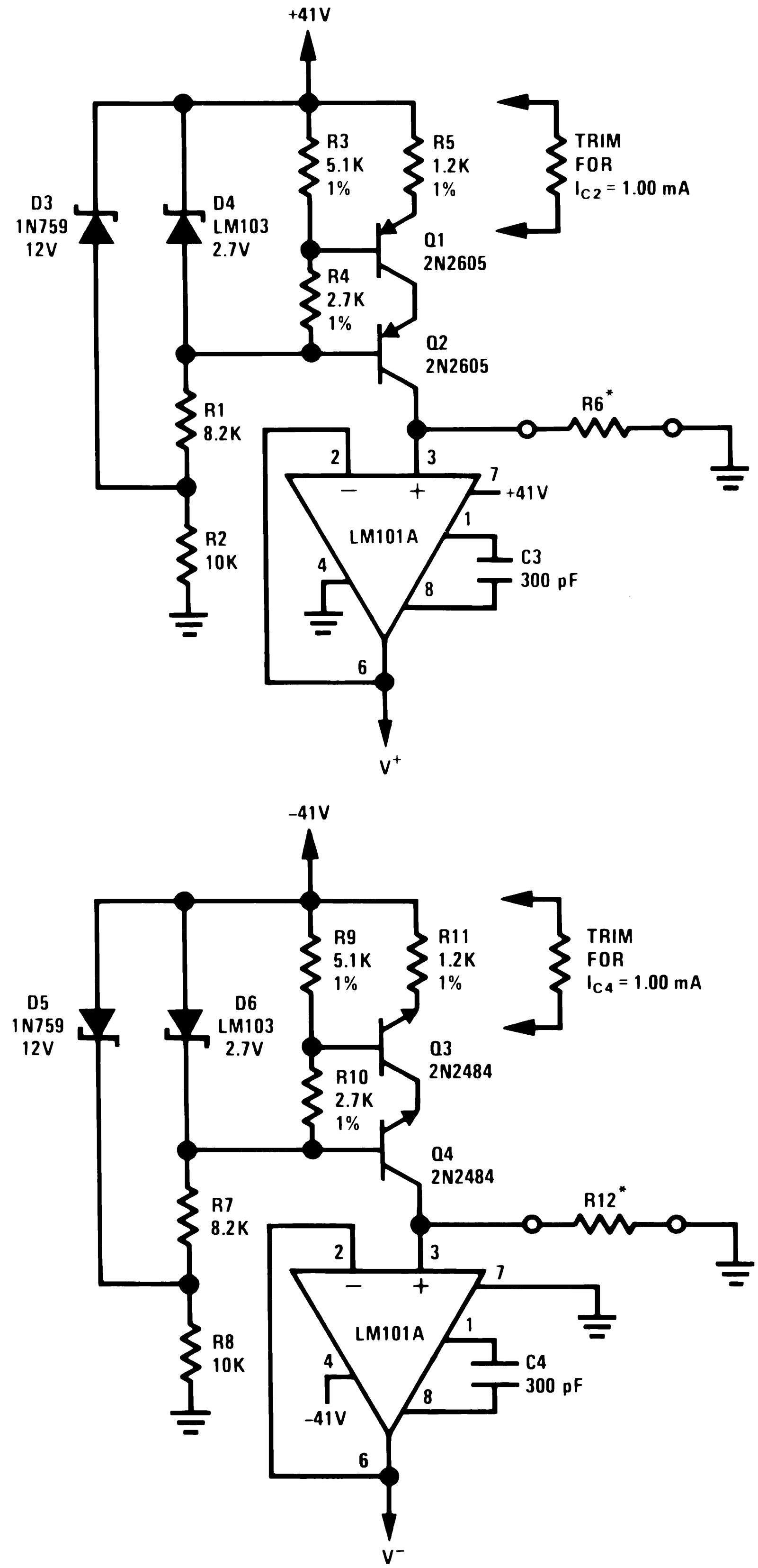


Figure 34. Wein Bridge Oscillator with FET Amplitude Stabilization



* V_{OUT} = 1V/kΩ

Figure 35. Low Power Supply for Integrated Circuit Testing

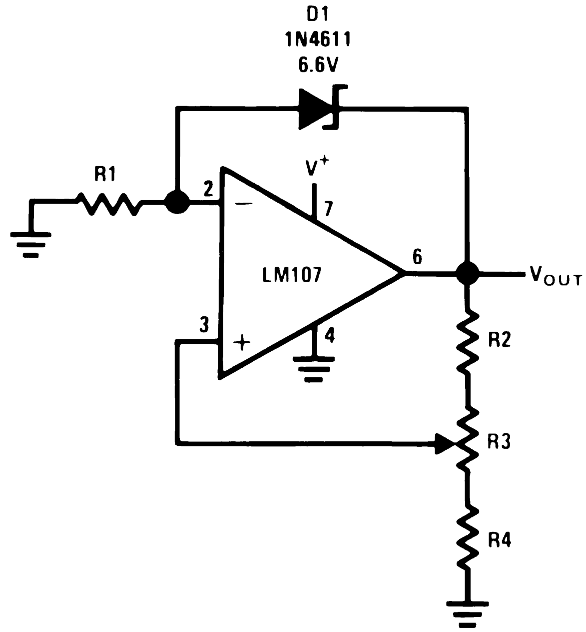


Figure 36. Positive Voltage Reference

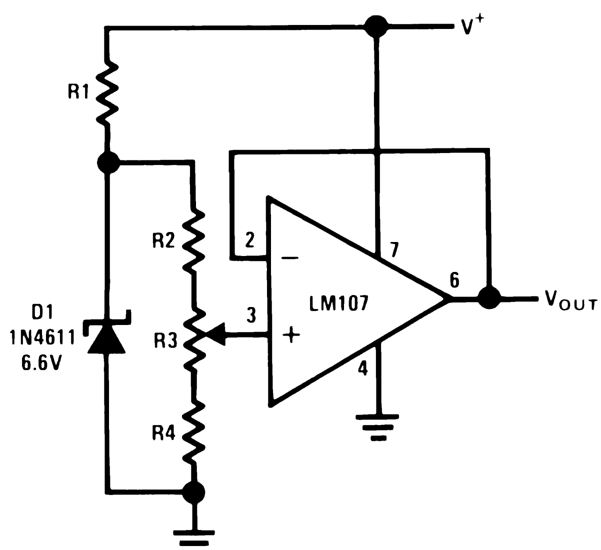


Figure 37. Positive Voltage Reference

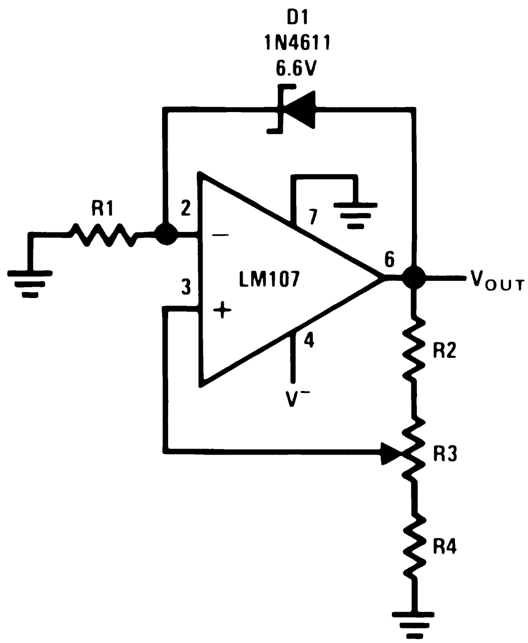


Figure 38. Negative Voltage Reference

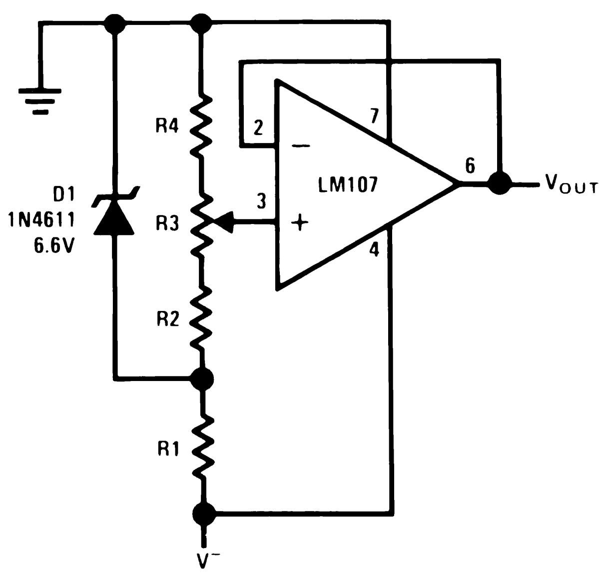


Figure 39. Negative Voltage Reference

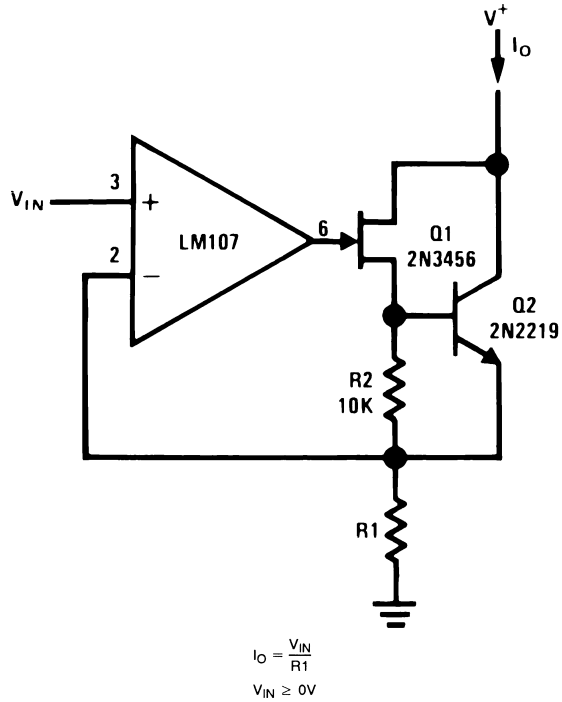


Figure 40. Precision Current Sink

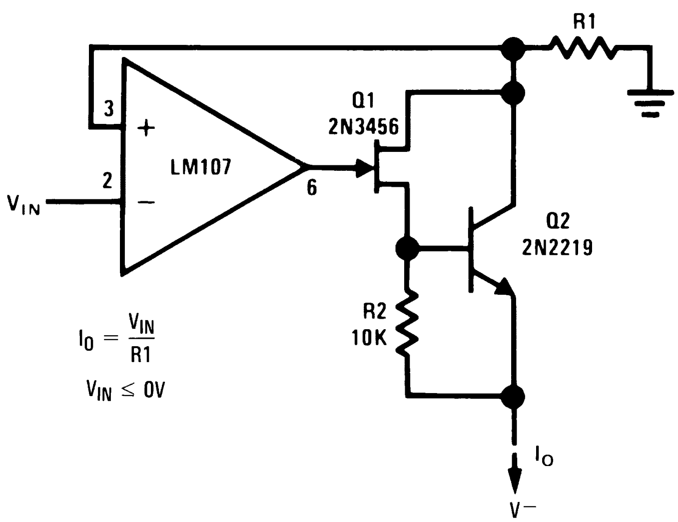
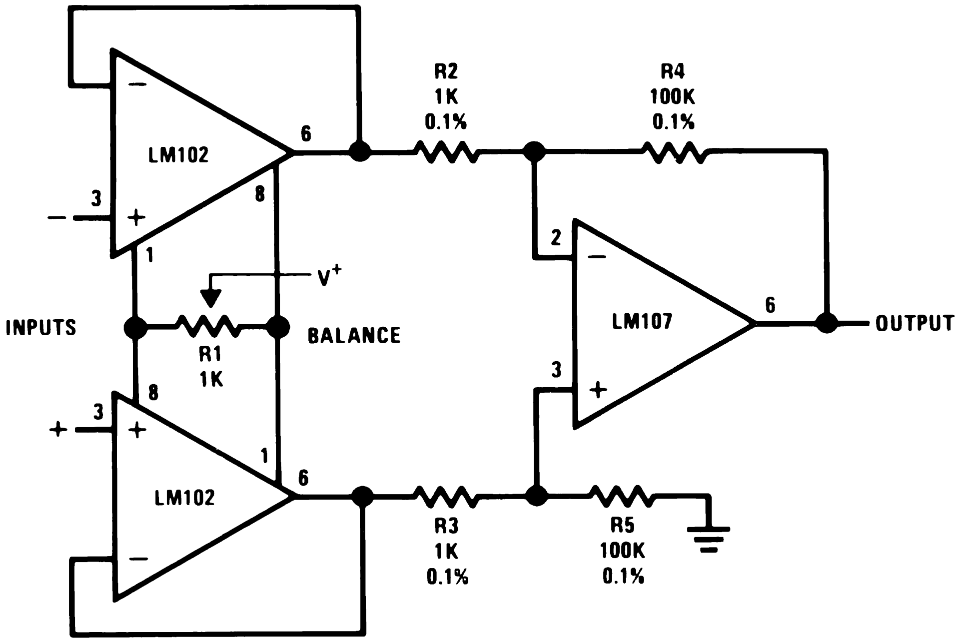


Figure 41. Precision Current Source

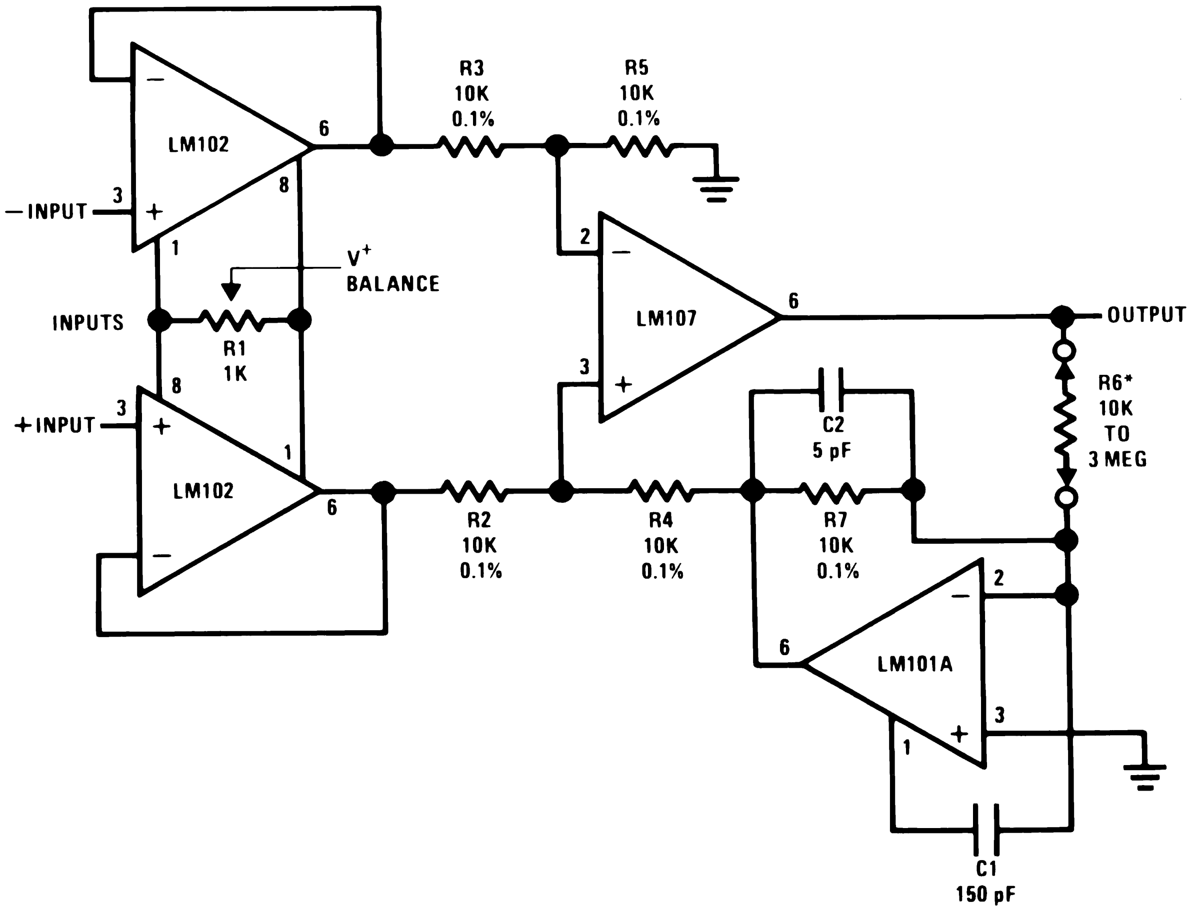
4 Signal Processing



$$\frac{R4}{R2} = \frac{R5}{R3}$$

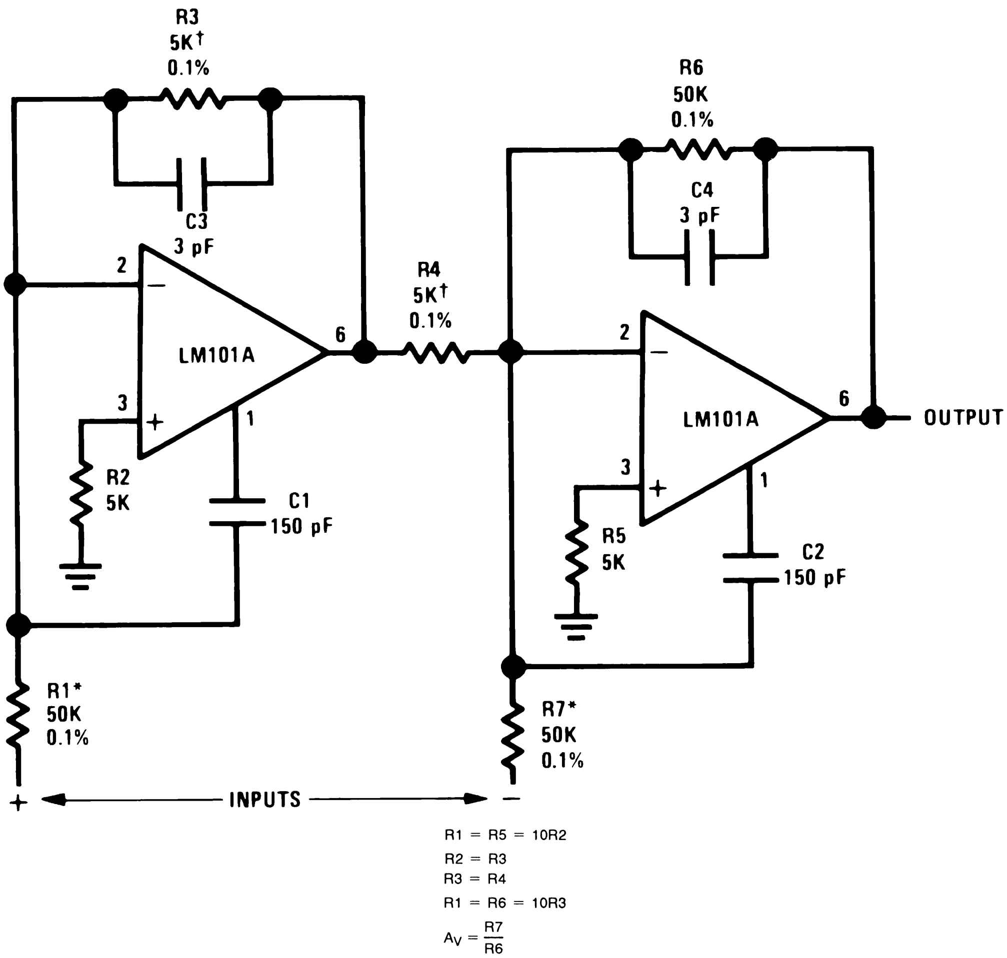
$$A_V = \frac{R4}{R2}$$

Figure 42. Differential-Input Instrumentation Amplifier



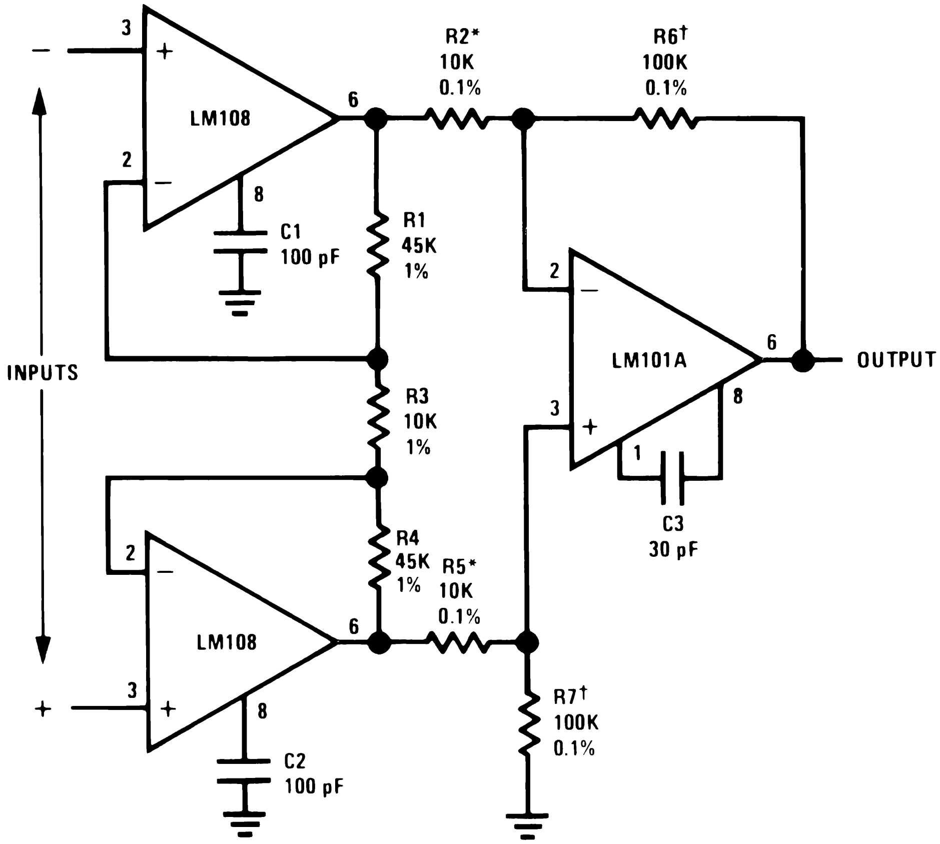
* Gain adjust $A_V = 10^{-4}$ R6

Figure 43. Variable Gain, Differential-Input Instrumentation Amplifier



† Matching determines common mode rejection.

Figure 44. Instrumentation Amplifier with ±100 Volt Common Mode Range



R1 = R4

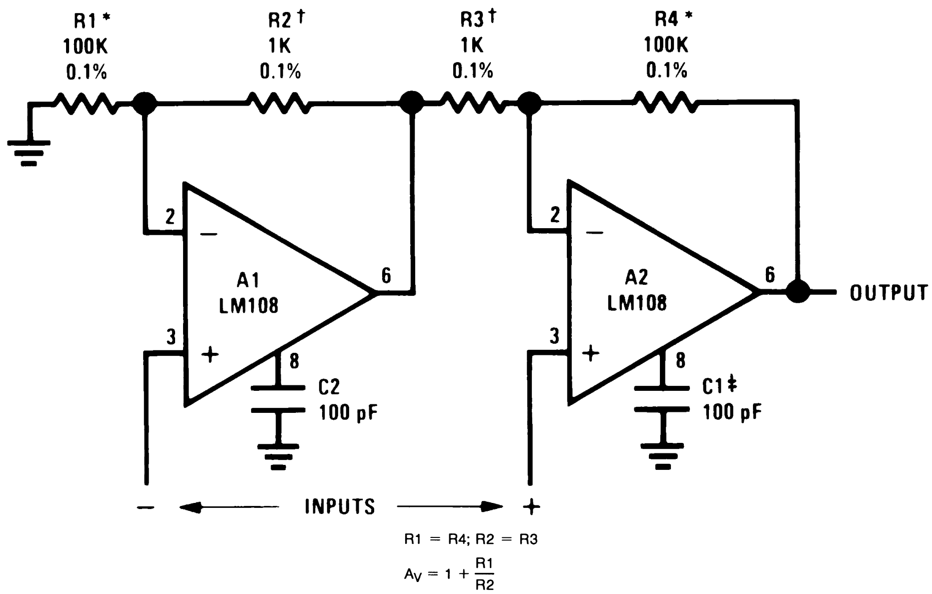
R2 = R5

R6 = R7

†*Matching Determines CMRR

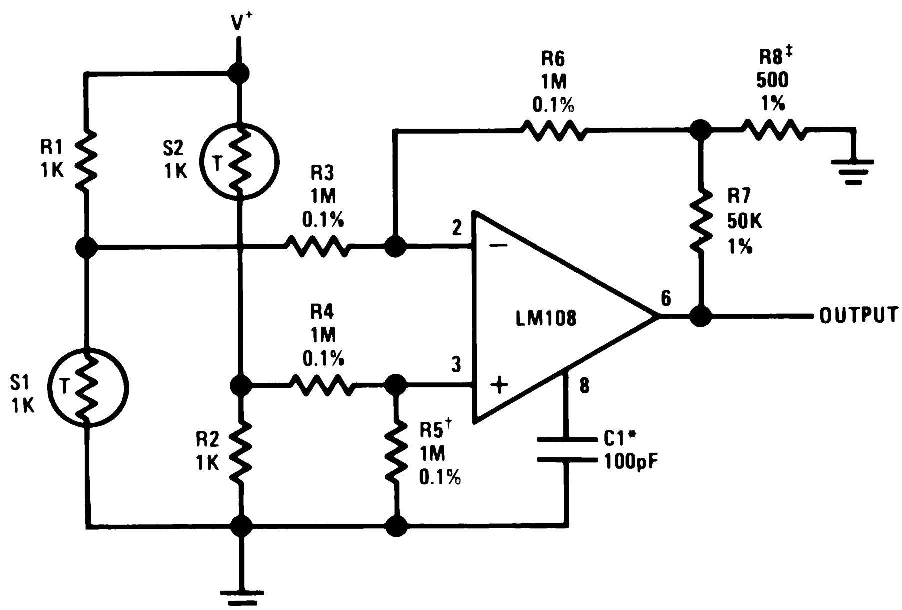
$$A_V = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right)$$

Figure 45. Instrumentation Amplifier with ±10 Volt Common Mode Range



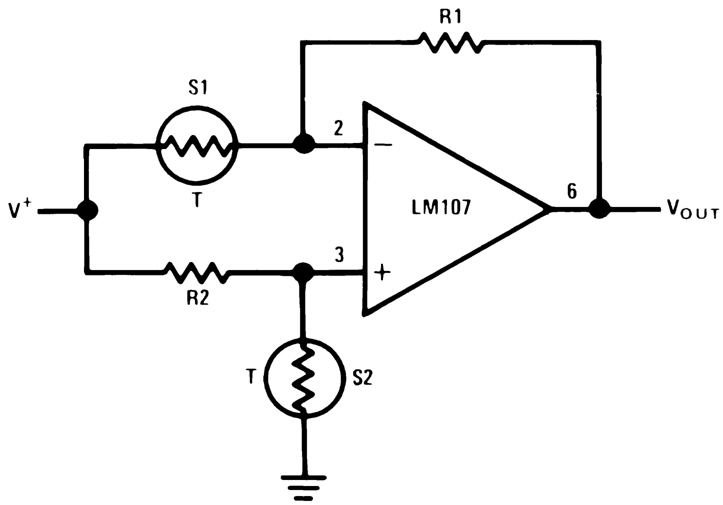
*† Matching Determines CMRR
‡ May be deleted to maximize bandwidth

Figure 46. High Input Impedance Instrumentation Amplifier



* Reduces feed through of power supply noise by 20 dB and makes supply bypassing unnecessary.
† Trim for best common mode rejection
‡ Gain adjust

Figure 47. Bridge Amplifier with Low Noise Compensation



$$\frac{R1}{R_{S1}} = \frac{R2}{R_{S2}}$$

$$V_{OUT} = V^{+}\left(1 - \frac{R1}{R_{S1}}\right)$$

Figure 48. Bridge Amplifier

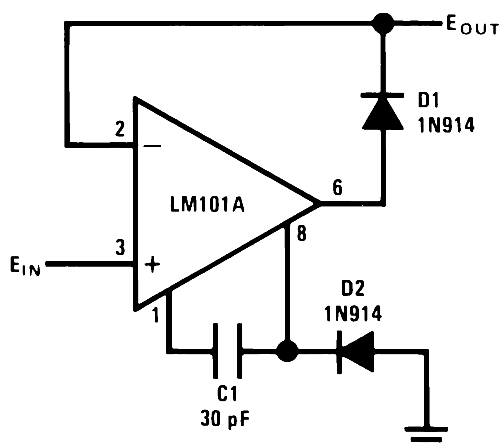
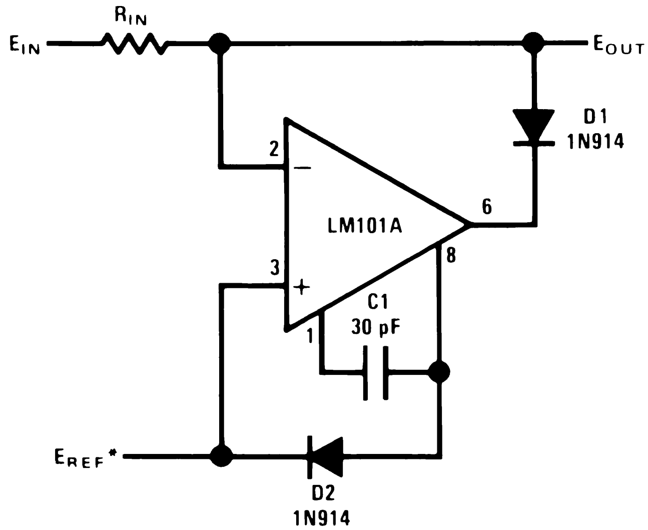


Figure 49. Precision Diode



* E_{REF} must have a source impedance of less than 200Ω if D2 is used.

Figure 50. Precision Clamp

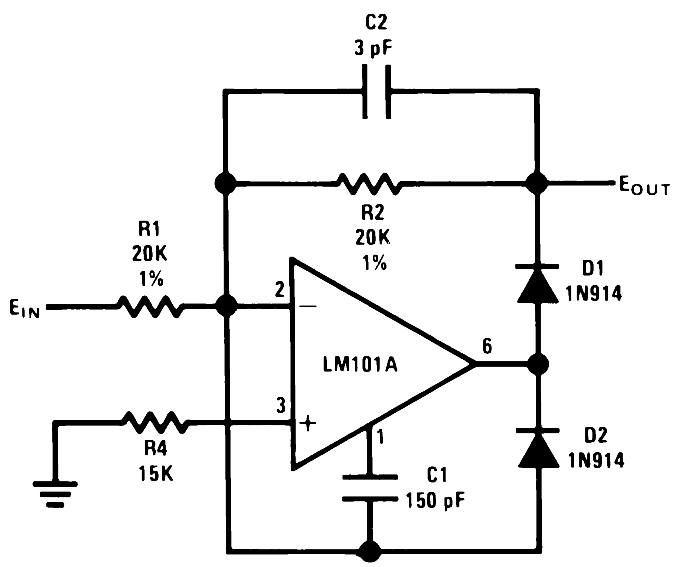
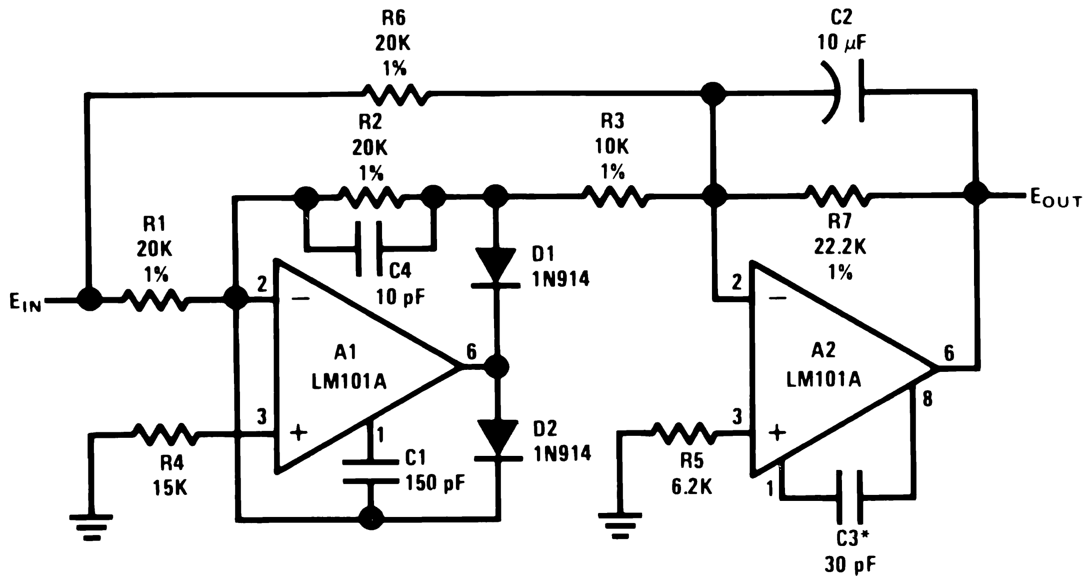


Figure 51. Fast Half Wave Rectifier



* Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Figure 52. Precision AC to DC Converter

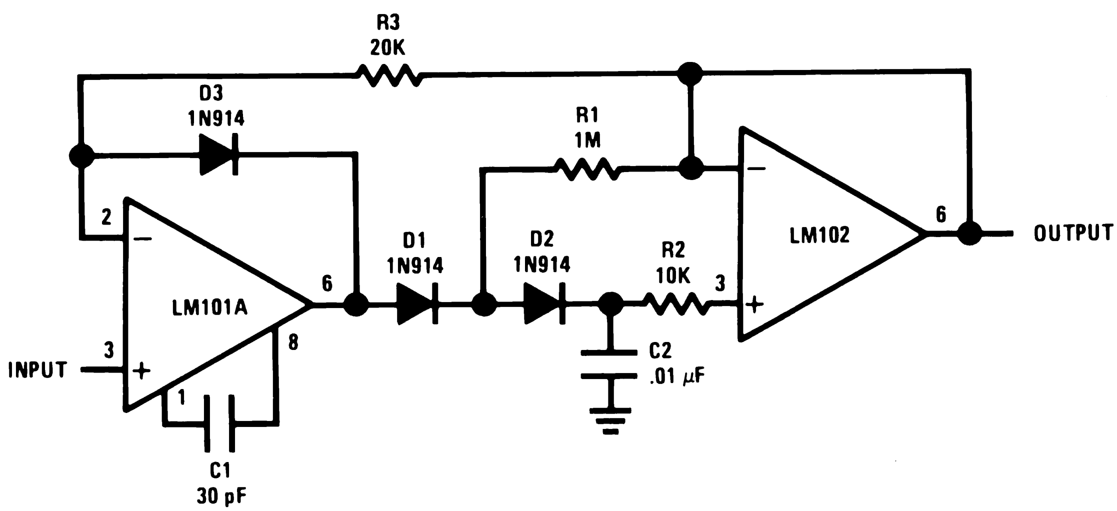
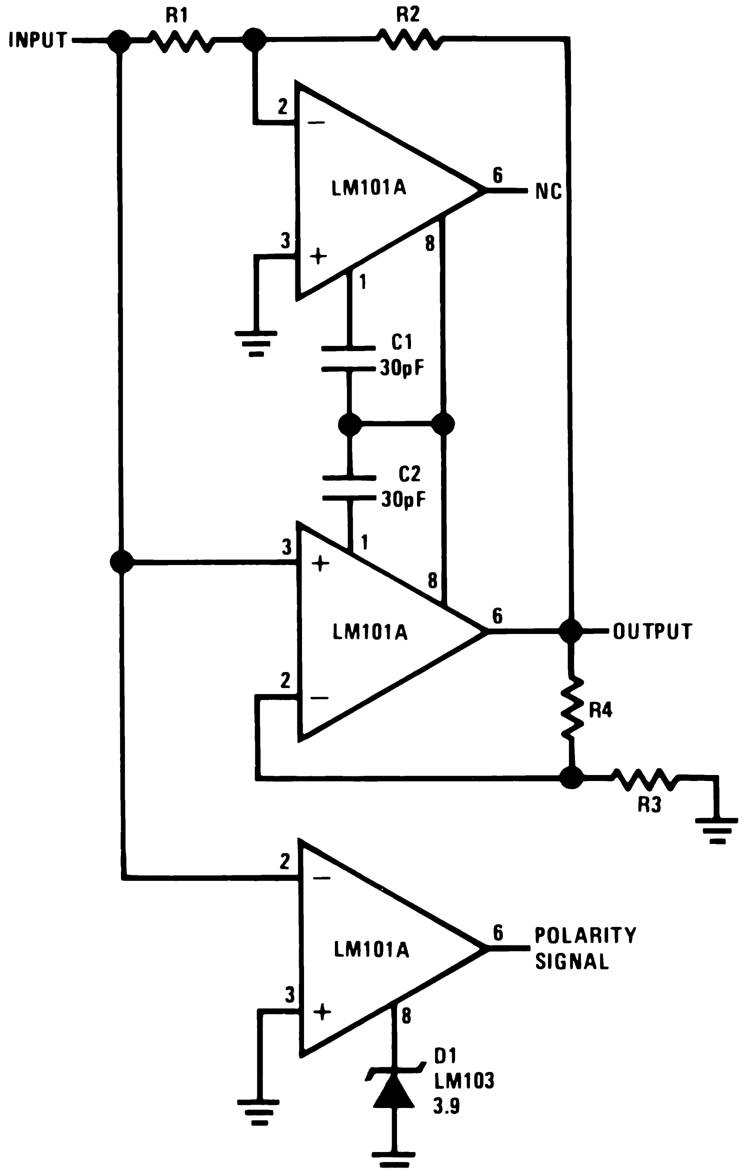


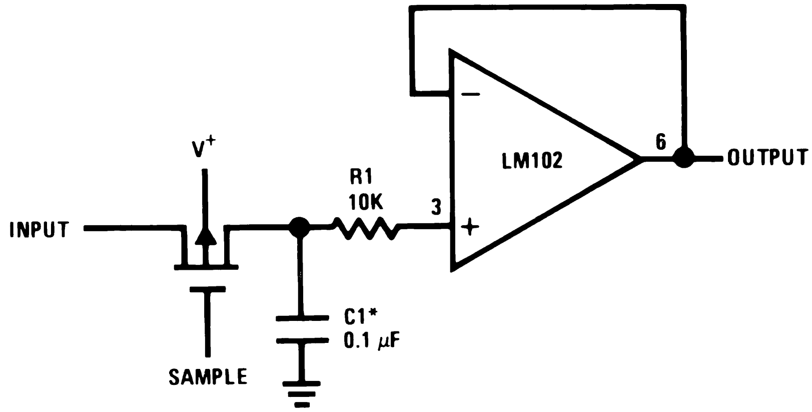
Figure 53. Low Drift Peak Detector



$$V_{OUT} = -|V_{IN}| \times \frac{R2}{R1}$$

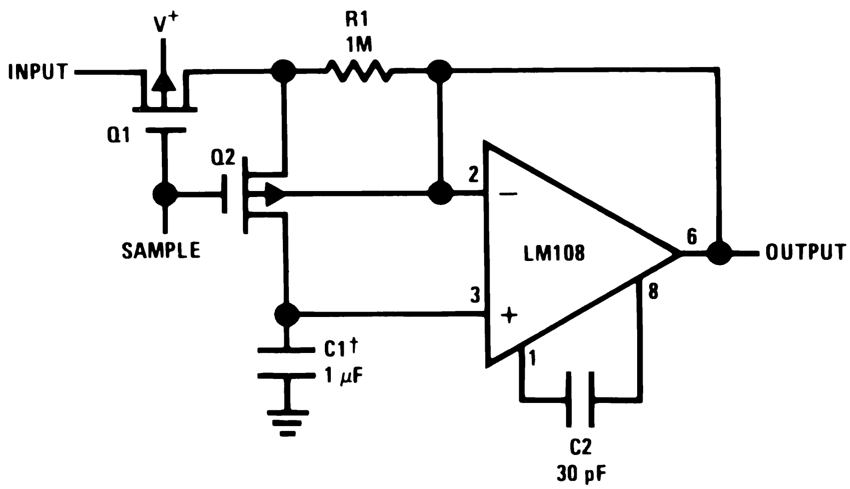
$$\frac{R2}{R1} = \frac{R4 + R3}{R3}$$

Figure 54. Absolute Value Amplifier with Polarity Detector



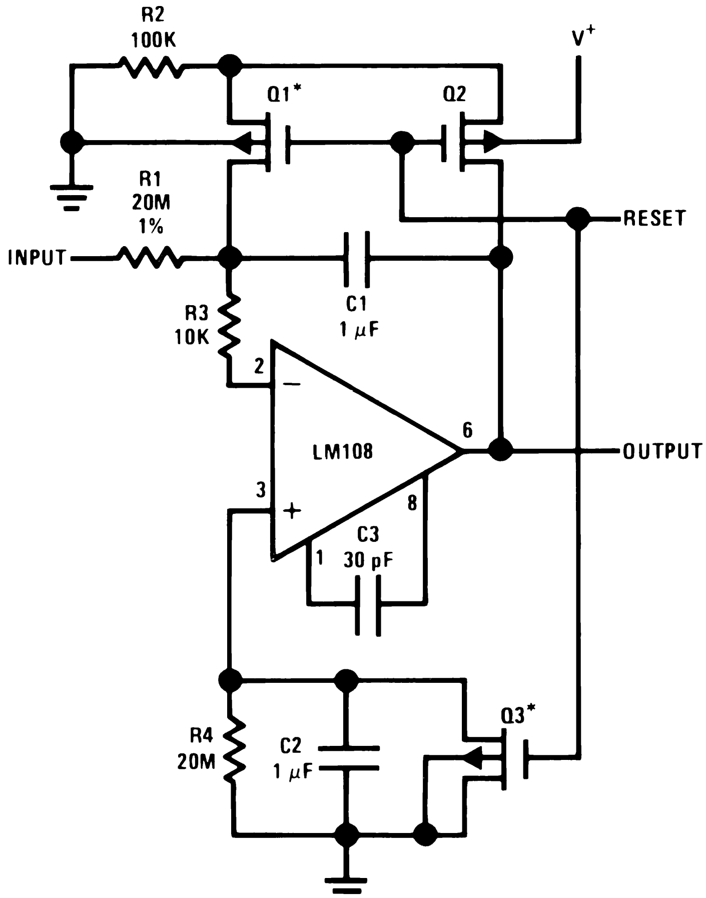
* Polycarbonate-dielectric capacitor

Figure 55. Sample and Hold



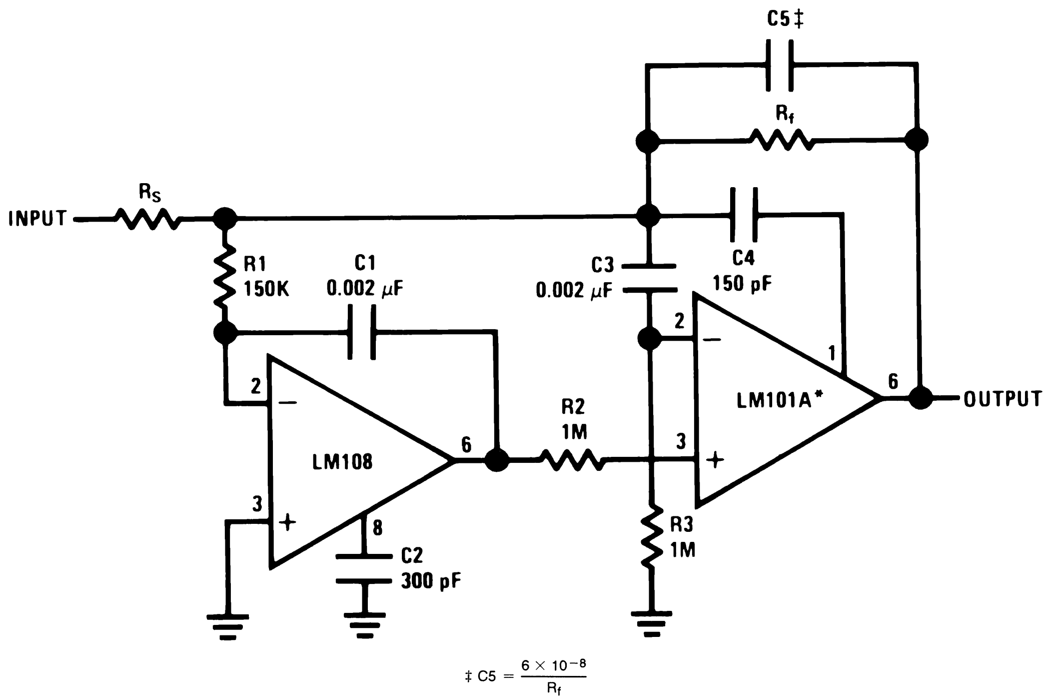
* Worst case drift less than 2.5 mV/sec
† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Figure 56. Sample and Hold



* Q1 and Q3 should not have internal gate-protection diodes.
Worst case drift less than 500 µV/sec over −55°C to +125°C.

Figure 57. Low Drift Integrator



* In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.
† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

Figure 58. Fast† Summing Amplifier with Low Input Current

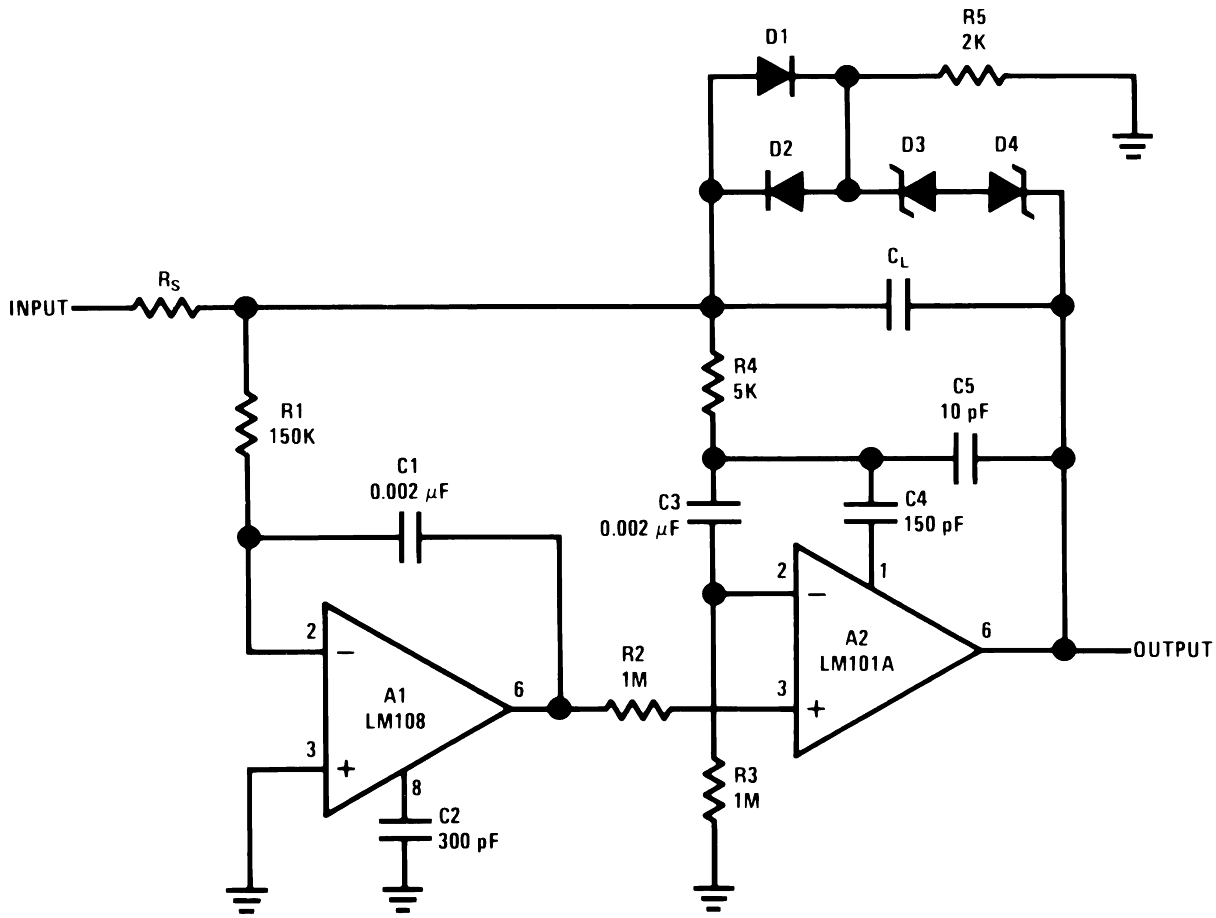
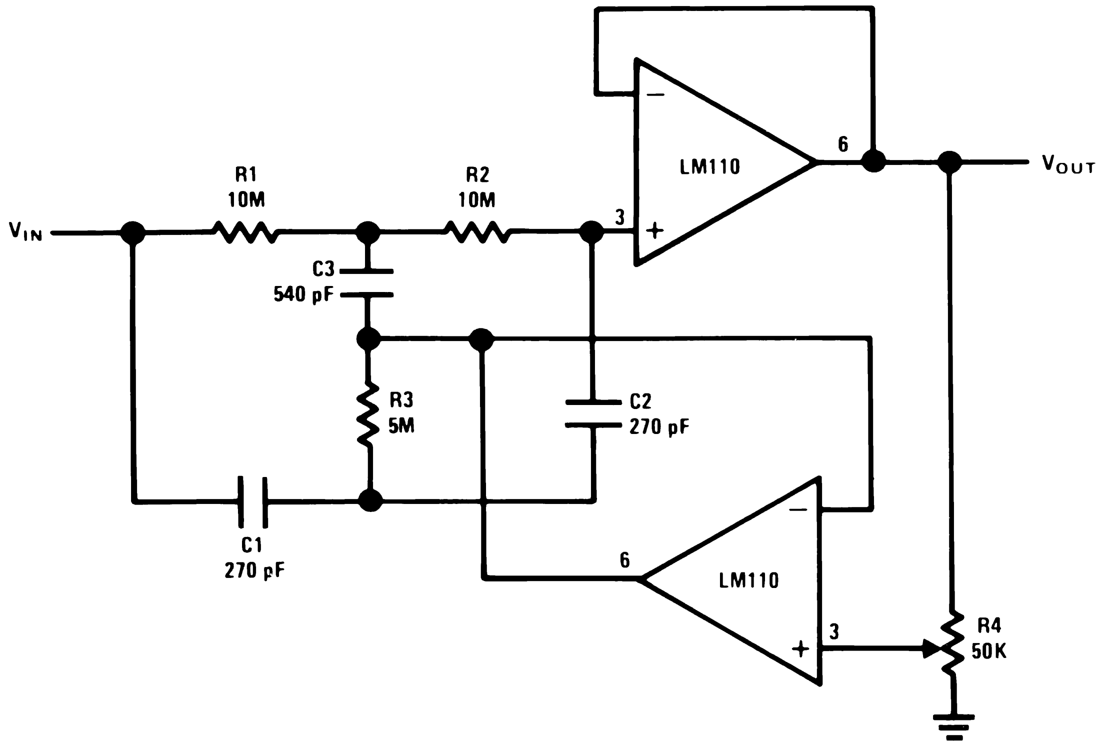
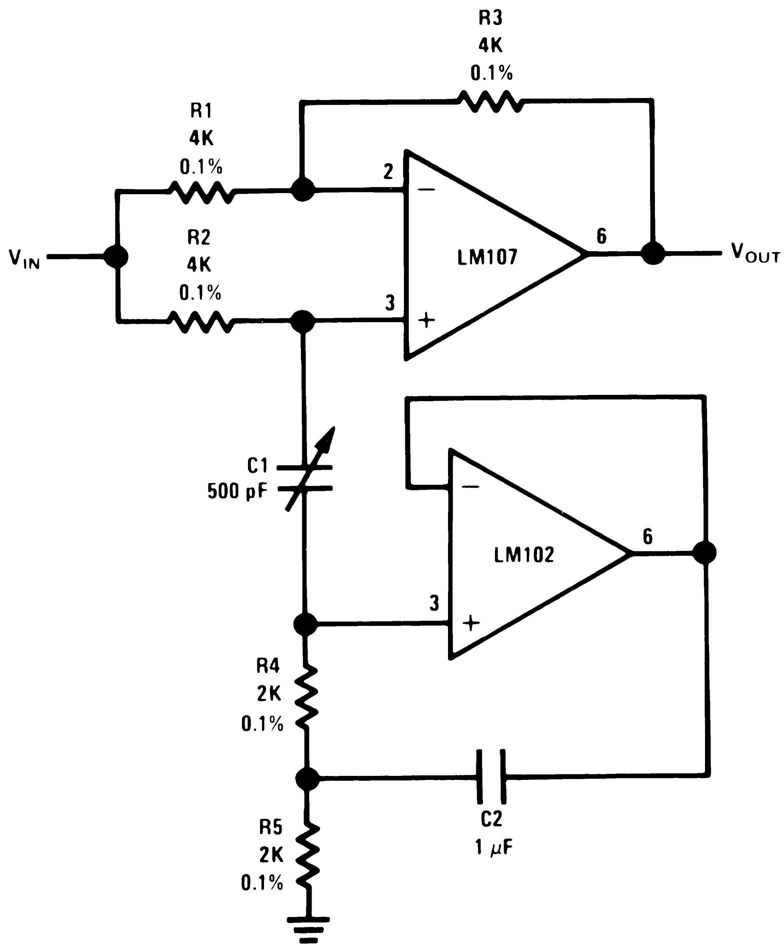


Figure 59. Fast Integrator with Low Input Current



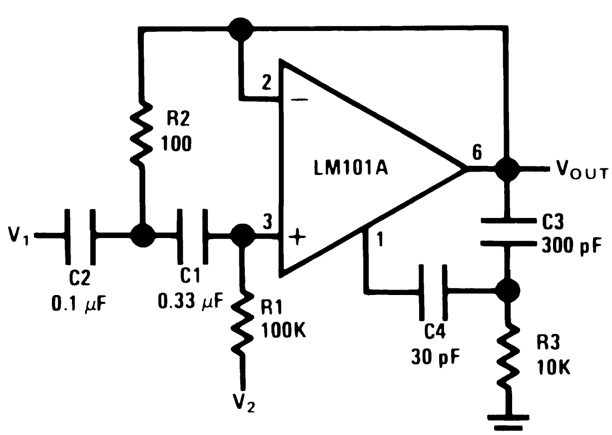
$$f_O = \frac{1}{2\pi R1C1}$$
$$= 60\ Hz$$
$$R1 = R2 = R3$$
$$C1 = C2 = C23$$

Figure 60. Adjustable Q Notch Filter



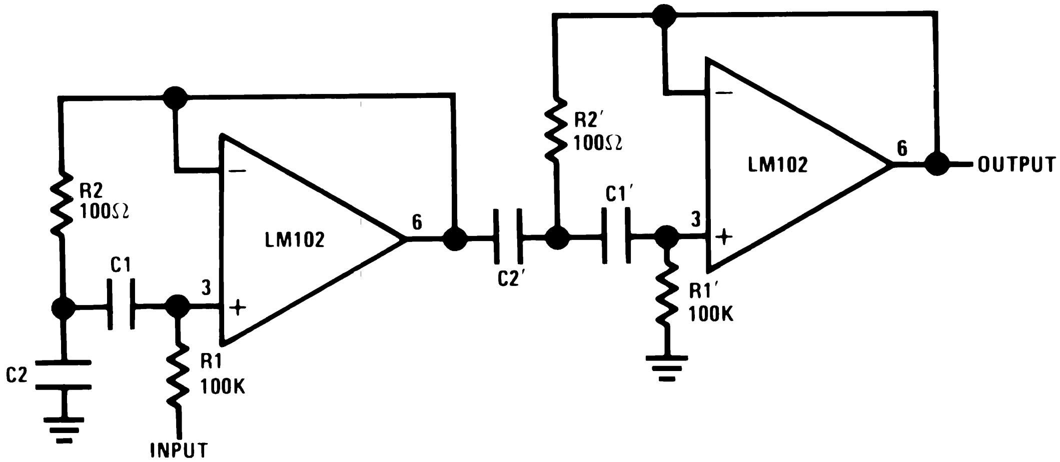
$$f_O = \frac{1}{2\pi R4\sqrt{C1C2}}$$

Figure 61. Easily Tuned Notch Filter



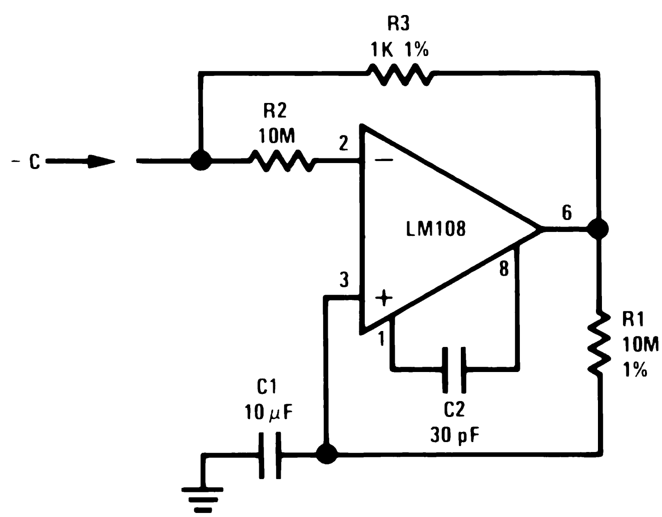
$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Figure 62. Tuned Circuit



$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Figure 63. Two-Stage Tuned Circuit

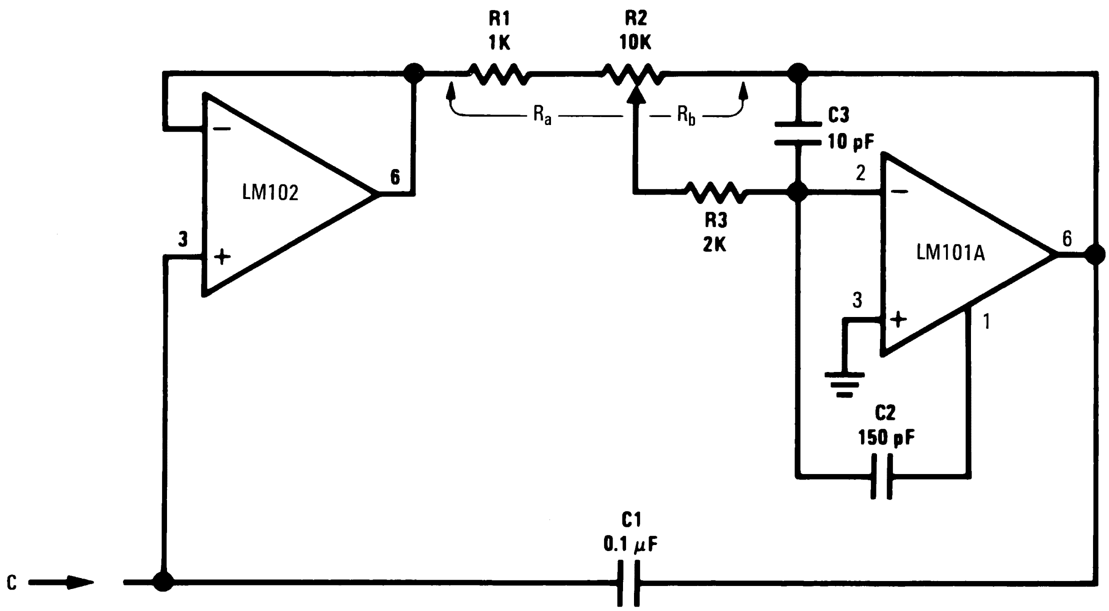


$$C = \frac{R2}{R3} C1$$

$$I_L = \frac{V_{OS} + R2\, I_{OS}}{R3}$$

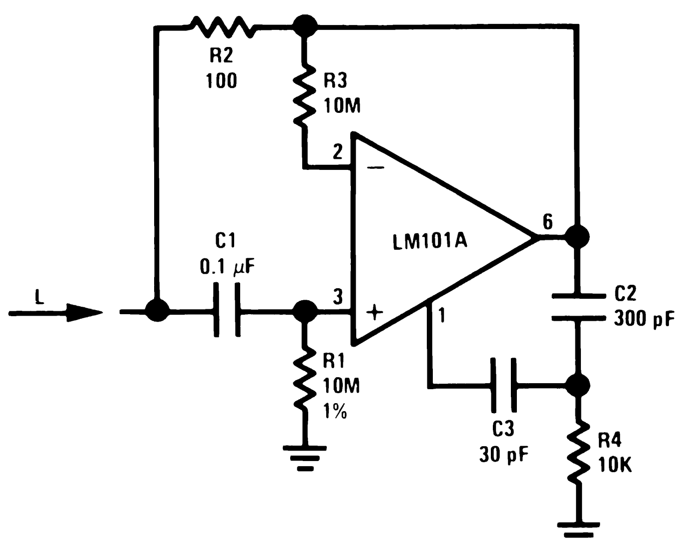
$$R_S = \frac{R3(R1 + R_{IN})}{R_{IN}\, A_{VO}}$$

Figure 64. Negative Capacitance Multiplier



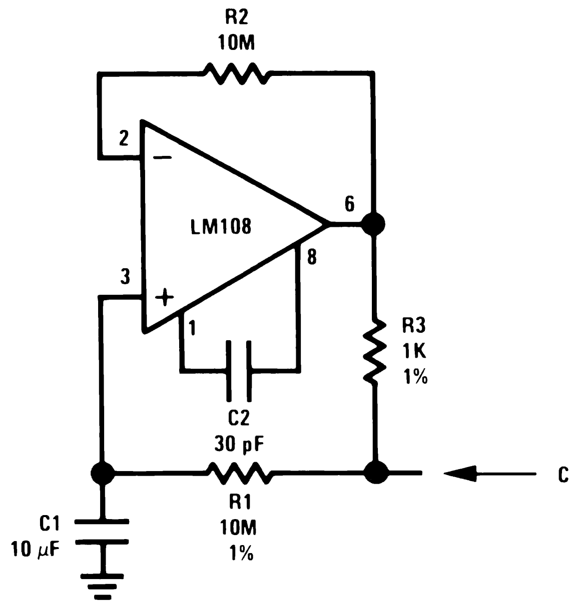
$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$

Figure 65. Variable Capacitance Multiplier



$L \geq R1\ R2\ C1$
$R_S = R2$
$R_P = R1$

Figure 66. Simulated Inductor

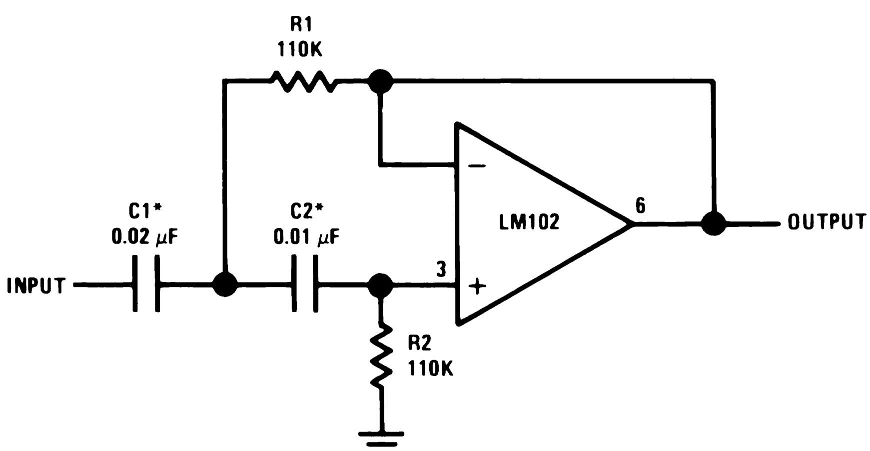


$$C = \frac{R1}{R3} C1$$

$$I_L = \frac{V_{OS} + I_{OS} R1}{R3}$$

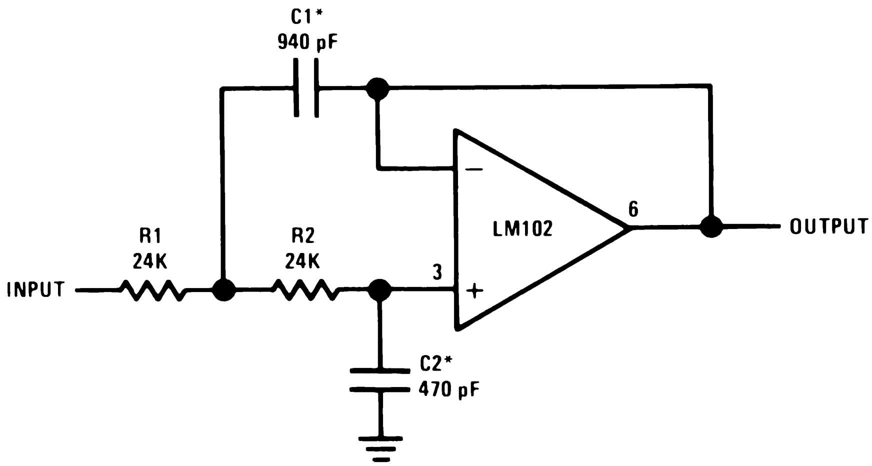
$$R_S = R3$$

Figure 67. Capacitance Multiplier



* Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

Figure 68. High Pass Active Filter



* Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

Figure 69. Low Pass Active Filter

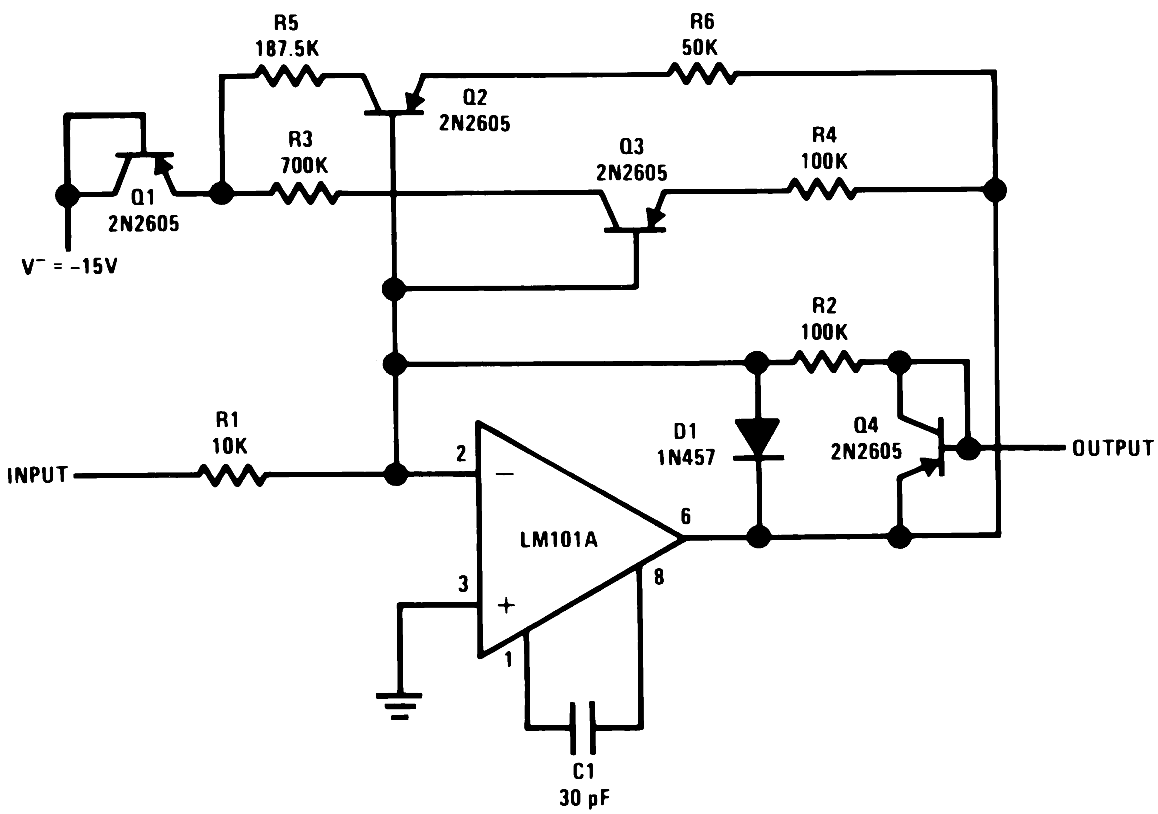
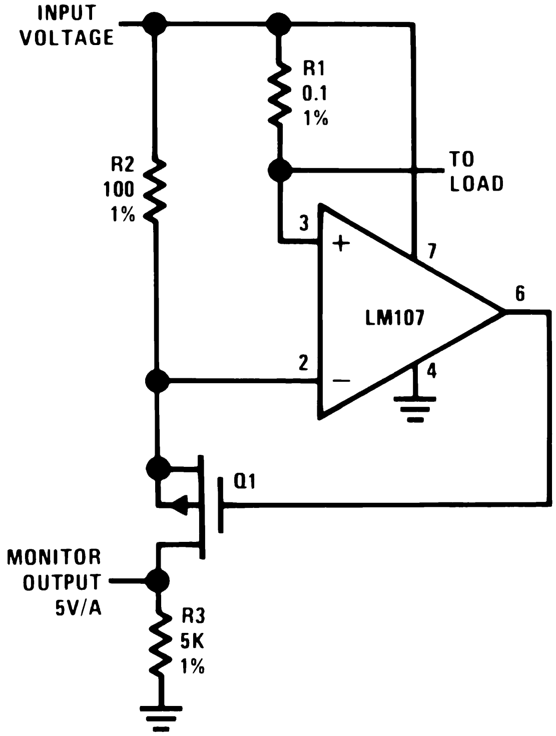


Figure 70. Nonlinear Operational Amplifier with Temperature Compensated Breakpoints



$$V_{OUT} = \frac{R1\ R3}{R2} I_L$$

Figure 71. Current Monitor

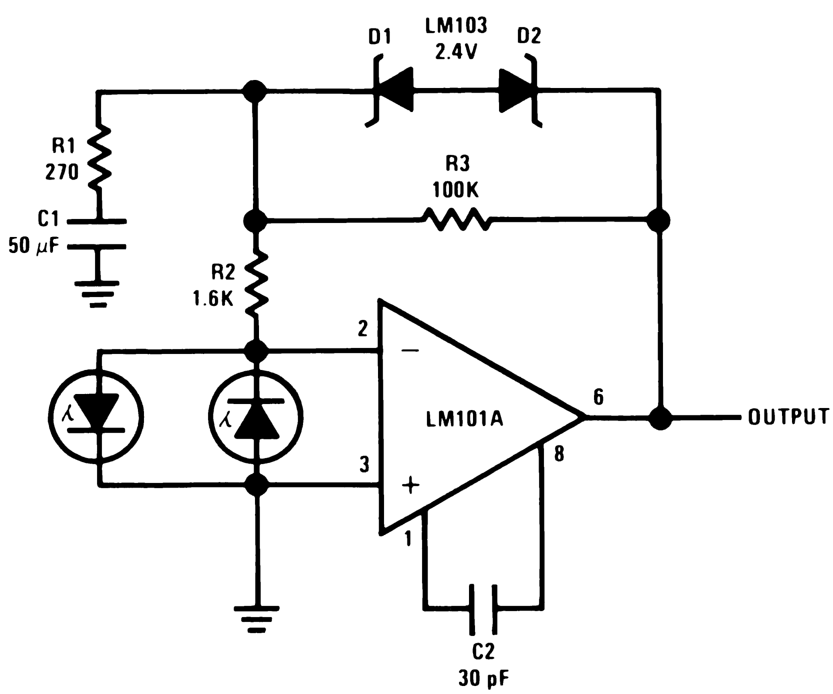


Figure 72. Saturating Servo Preamplifier with Rate Feedback

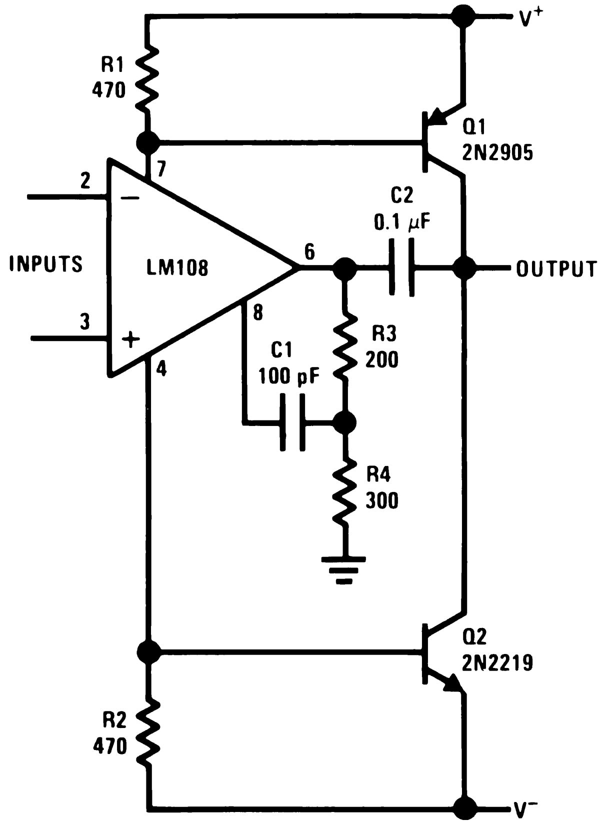
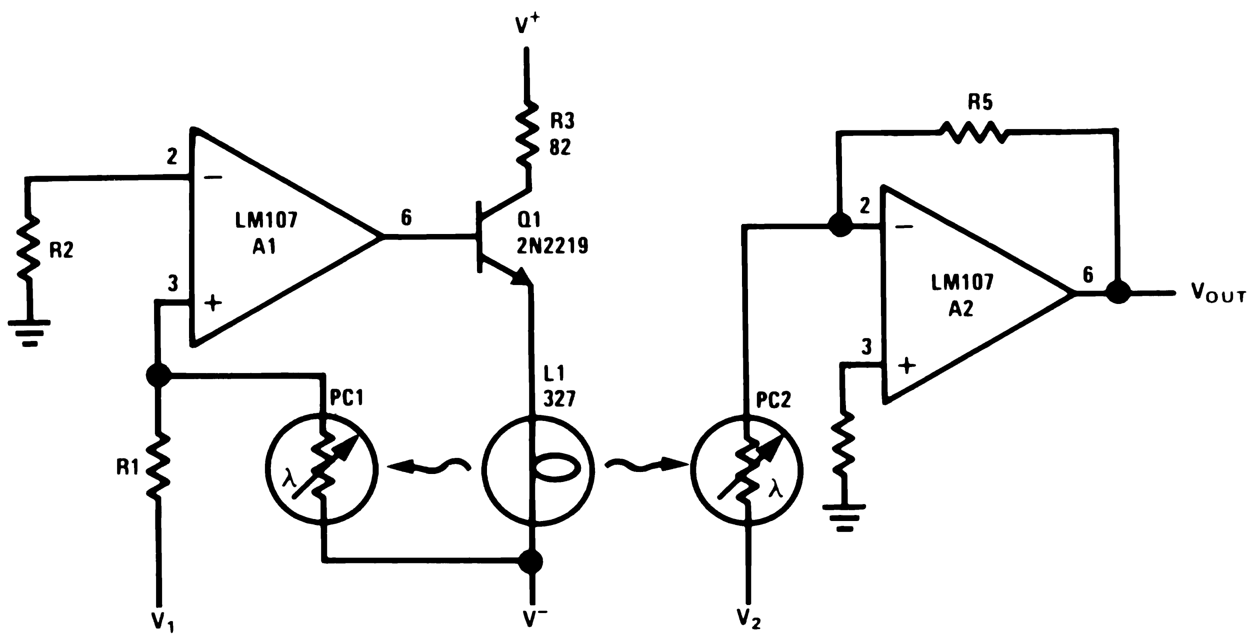


Figure 73. Power Booster

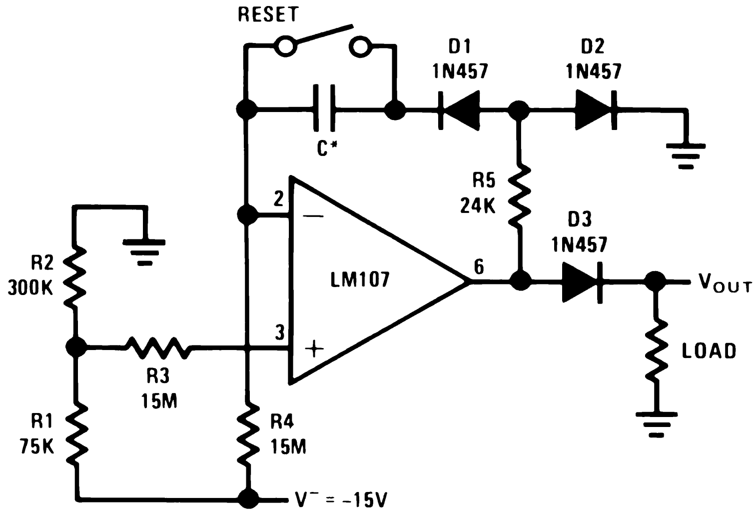


$$R5 = R1\left(\frac{V^-}{10}\right)$$

$$V_1 \geq 0$$

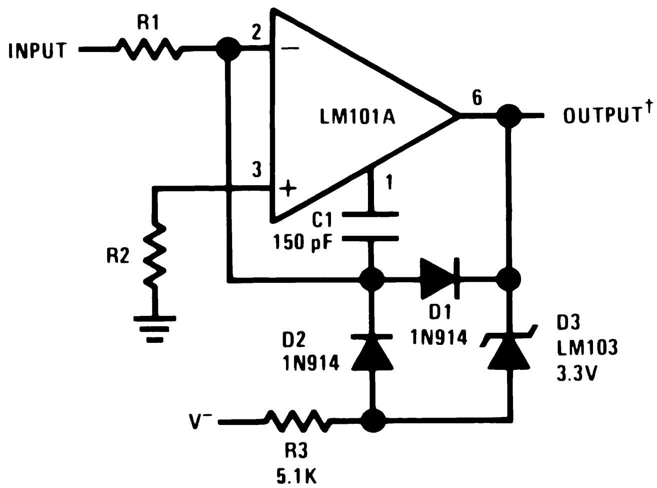
$$V_{OUT} = \frac{V_1 V_2}{10}$$

Figure 74. Analog Multiplier



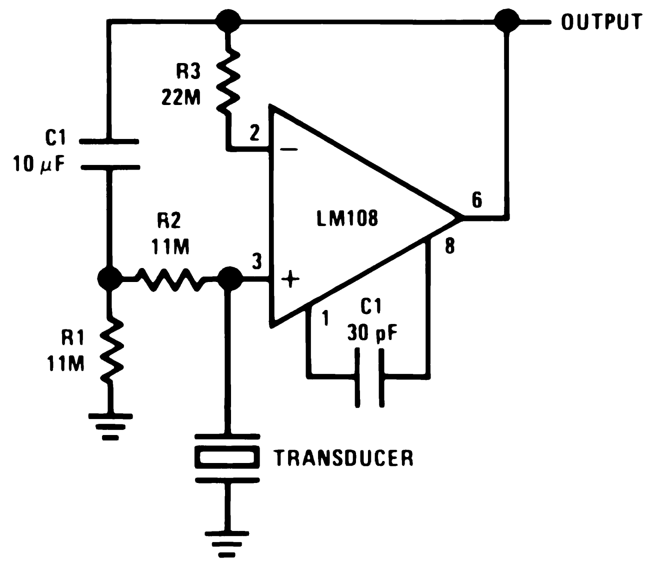
* Low leakage −0.017 μF per second delay

Figure 75. Long Interval Timer



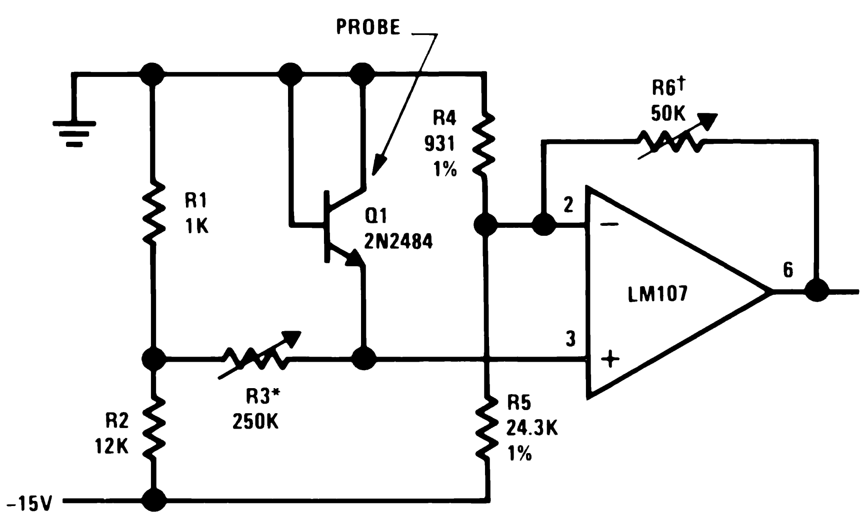
Propagation delay approximately 200 ns
† DTL or TTL fanout of three.
Minimize stray capacitance
Pin 8

Figure 76. Fast Zero Crossing Detector



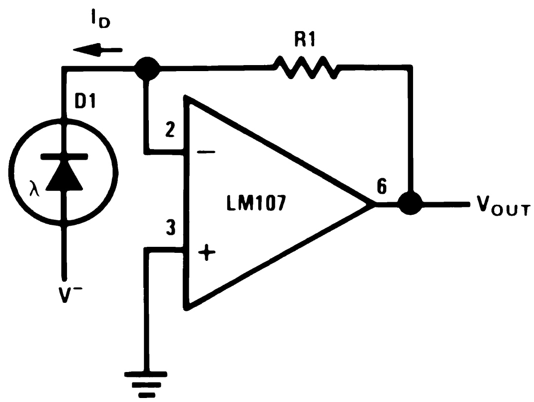
Low frequency cutoff = R1 C1

Figure 77. Amplifier for Piezoelectric Transducer



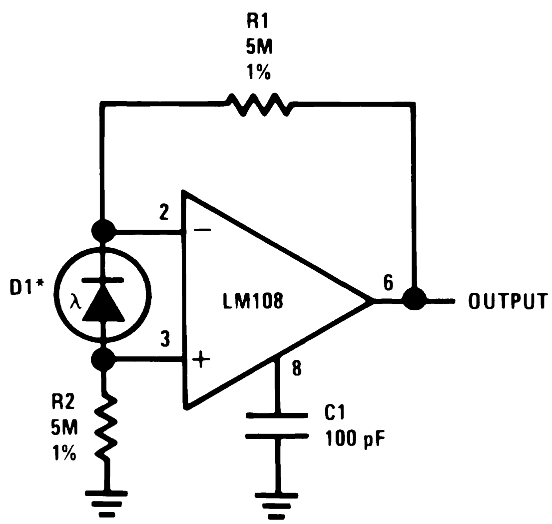
* Set for 0V at 0°C
† Adjust for 100 mV/°C

Figure 78. Temperature Probe



$V_{OUT} = R1\ I_D$

Figure 79. Photodiode Amplifier



$V_{OUT} = 10\ V/\mu A$

*Operating photodiode with less than 3 mV across it eliminates leakage currents.

Figure 80. Photodiode Amplifier

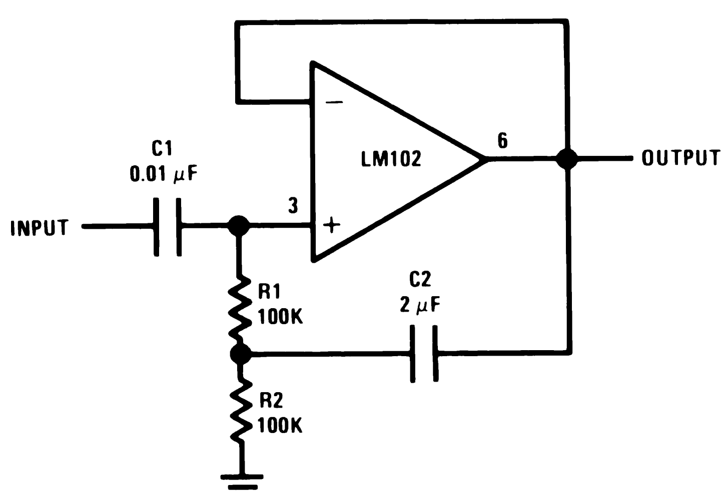
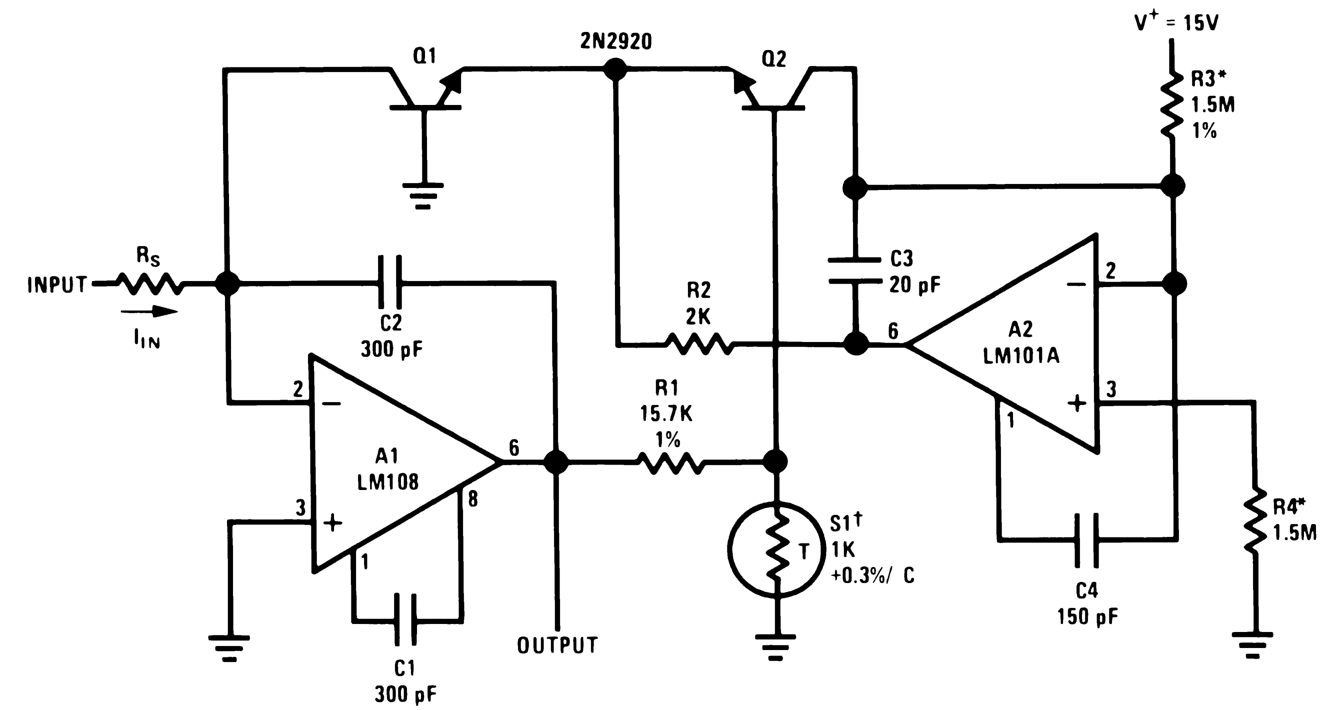
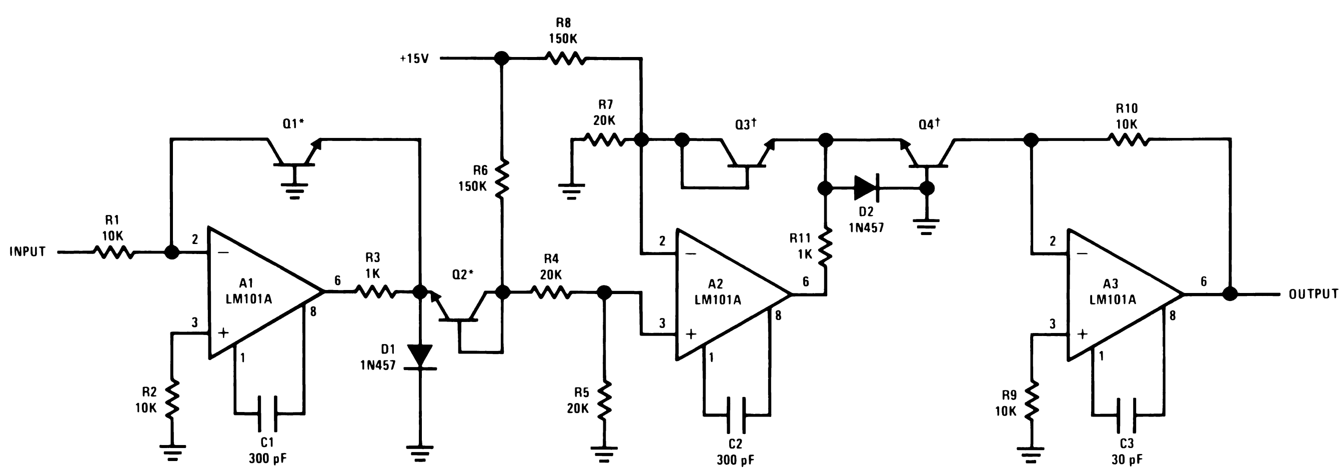


Figure 81. High Input Impedance AC Follower



10 nA < I_{IN} < 1 mA
Sensitivity is 1V per decade
† 1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.
* Determines current for zero crossing on output: 10 μA as shown.

Figure 82. Temperature Compensated Logarithmic Converter



*† 2N3728 matched pairs

Figure 83. Root Extractor

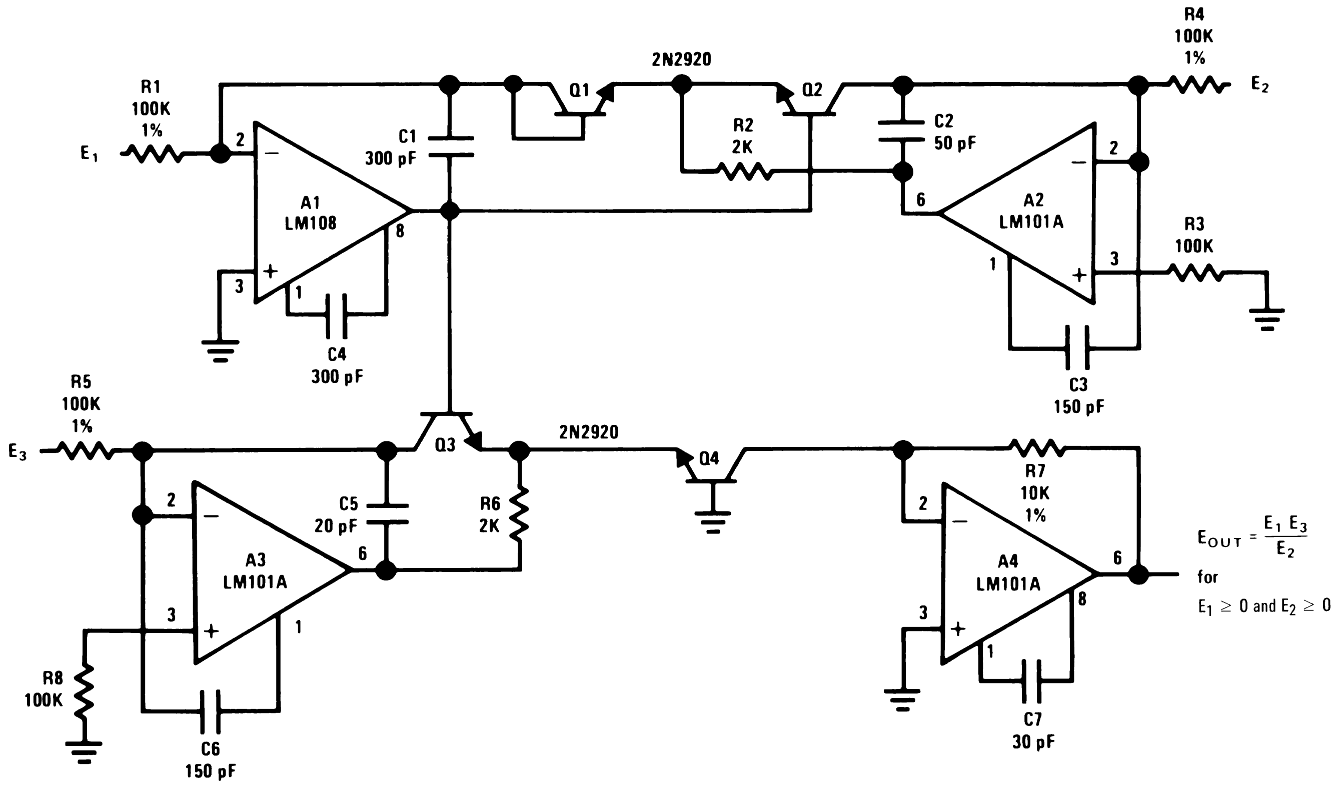


Figure 84. Multiplier/Divider

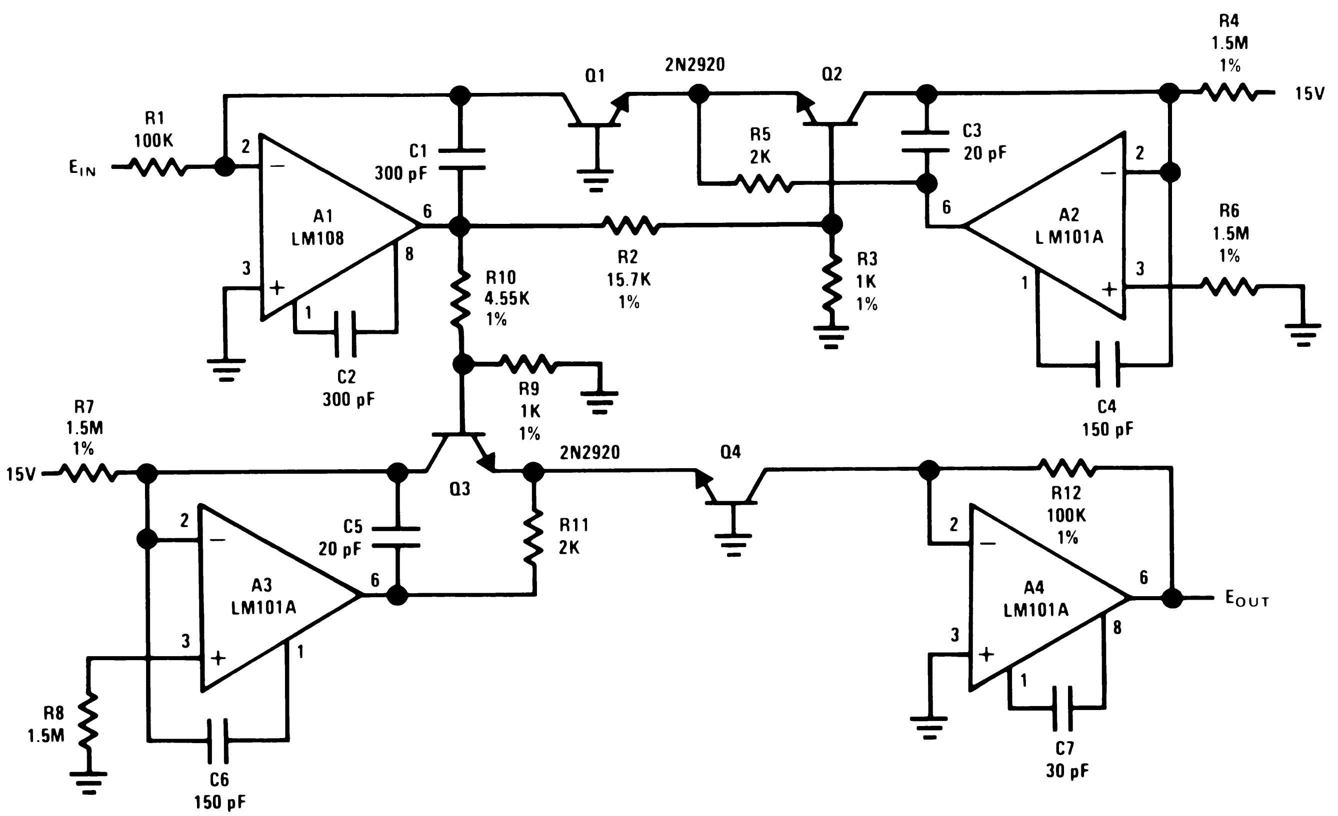
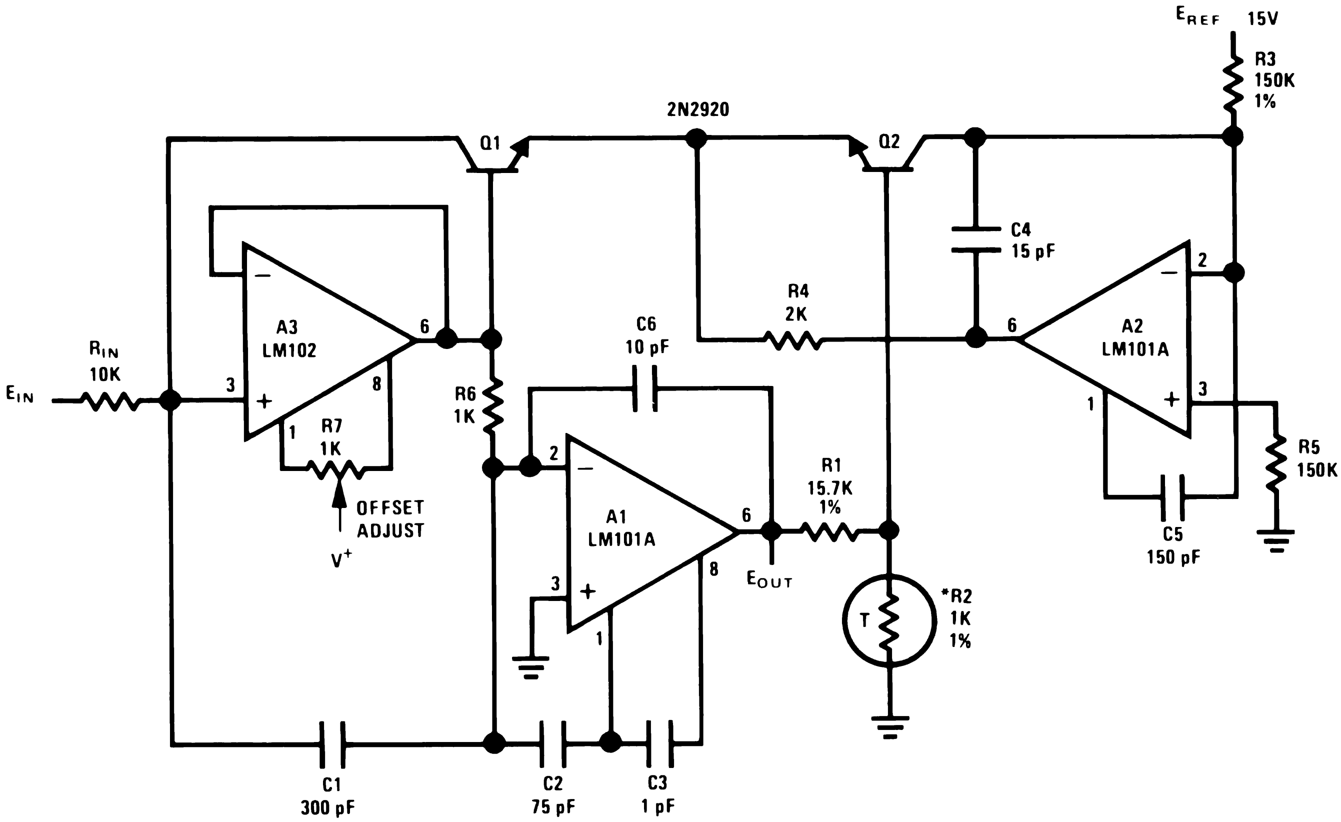
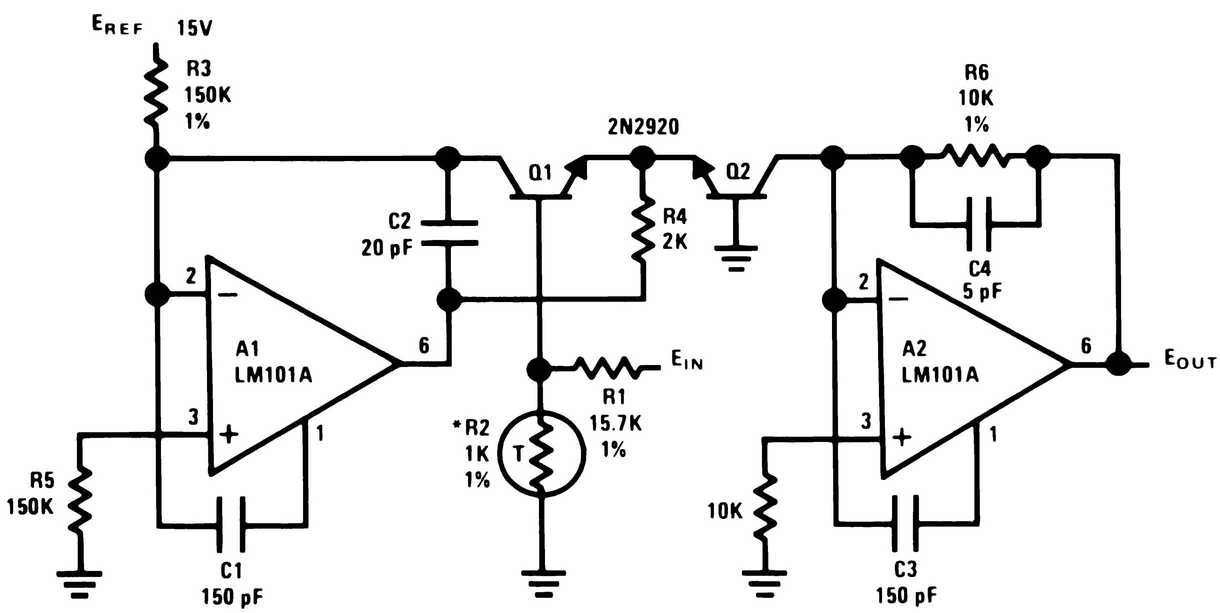


Figure 85. Cube Generator



† 1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

Figure 86. Fast Log Generator



† 1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

Figure 87. Anti-Log Generator

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